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Work type : RES
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PROJECT ADMINISTRATION DATA

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SR-854

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NOTICE OF PROJECT CLOSEOUT

Date 3/8/89

Project No. E-21-636 Center No. R6419-0A0

Project Director P. E. Allen School/Lab EE

Sponsor Semiconductor Research Corporation

Contract/Grant No. 87-DJ-091 GTRC XX GIT ____

Prime Contract No. ____

Title Analog CAD Methodology

Effective Completion Date 8/31/88 (Performance) 10/31/88 (Reports)

Closeout Actions Required:

X None
____ Final Invoice or Copy of Last Invoice - Already Submitted.
____ Final Report of Inventions and/or Subcontracts
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____ Classified Material Certificate
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Schlumberger Professor

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Georgia Institute of Technology
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ABSTRACT OF CONTENTS OF THIS SUBMISSION (must be in the space below or on a separate sheet of paper attached to this form)

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodology" from September 1, 1987 to November 31, 1987. It involves the research progress of 8 PhD students and 1 MS student. Primary results include the completion of the AIDE2 programmers manual, further measurements of AIDE2 designed circuits, development of a modeling capability for GB, PSRR, and noise in switched capacitor circuits, a comparison of the table look-up model with BSIM and SPICE level 2 models for a CMOS inverter, the evaluation of an 8-bit converter designed by ADDAC, development of a program to generate circuit implementations of a general frequency independent two-port transfer function, and the development of functional macromodels for various complex analog nonlinear circuits.

If an abstract of this paper has already been submitted to the SRC for approval, please check the box and give the SRC Publication ID number, if known. [ ] Abstract was previously submitted SRC Publication ID_____

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)

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SRC COOPERATIVE RESEARCH

SRC TECHNICAL THESAURUS

Circle at least one (1) word from List A and no more than the six (6) most appropriate words from List B

LIST A

ANALOG
BIPOLAR
CAD
CMOS
COMPUTING ARRAYS
DESIGN STYLES
DESIGN/ARCHITECTURE
DIGITAL
GAAS DEVICES/PROCESSES
INTERCONNECTIONS/CONTACTS
MANUFACTURING AUTOMATION
MANUFACTURING SCIENCE
MODELING/SIMULATION
MOSFET
OPTOELECTRONIC
PACKAGING
RELIABILITY
SILICON PROCESSES
SOFTWARE
SYNTHESIS
VERIFICATION

LIST B

3-D VLSI
A/D CONVERTER
ACOUSTIC MICROSCOPY
ALGORITHM
AMORPHOUS
ANALYTICAL MODELING
ANALYTICAL/EMPIRICAL MODELING
ANISOTROPIC ETCHING
ANNEALING
ARRAY LOGIC
ARTIFICIAL INTELLIGENCE
AUGER
AUTOMATED LAYOUT
AUTOMATION
BUILDING BLOCK LAYOUT
CAM
CARRIER FREEZE-OUT
CATASTROPHIC FAILURES
CERAMIC SUBSTRATES
CHANNEL ROUTER
CHARGE INJECTION
CIRCUIT ANALYSIS
CIRCUIT SIMULATION
CLEANING
CLUSTER ION BEAMS
COMPACTION
COMPILATION
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DATA MANAGEMENT
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DESIGN CONCEPTS
DESIGN INTERCHANGE FORMAT
DESIGN VERIFICATION
DESIGN-FOR-TEST
DEVICE DESIGN
DEVICE MODELING
DEVICE STRUCTURE
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DIGITAL IMAGING TECHNIQUES
DRAM
E-BEAM
ELECTROMIGRATION
ELECTROSTATIC DISCHARGE
EMITTERS
EPILAYERS
EQUIPMENT MODELS
ERROR CHECKING
ETCHING
EXPERT SYSTEMS
FABRICATION
FAILURE MECHANISMS
FAULT MODELS
FAULT SIMULATION
FAULT TOLERANCE
FAULTS
FILMS
FLEXIBLE CAM
FLOOR PLANNING
FLOORPLAN
FOCUSED ION BEAM
GAAS
GATE ARRAY
GATE MATRIX
GATE OXIDES
GATE-LEVEL SIMULATION
GETTERING
GRAPH THEORY
GRAPHICS
HARDWARE DESCRIPTION LANGUAGE
HEAT TRANSFER
HEMT
HETEROJUNCTION
HETEROSTRUCTURE
HIERARCHY
HOT-CARRIER
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IC/CAD TOOLS
IMAGE PROCESSING
IMPLANTATION
IN SITU PROCESS
IN-PROCESS
INSULATOR
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ION MILLING
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LASER ETCHING
LASER PHOTOCHEMISTRY
LATCHUP
LAYOUT TOOL
LAYOUT
LISP
LITHOGRAPHY
LOGIC OPTIMIZATION
LOGIC SIMULATION
LOW TEMPERATURE
LOW-TEMPERATURE EPITAXY
LPCVD
MACHINE VISION
MASK
MBE
MESFETS
METROLOGY
MISFIT DISLOCATIONS
MODFET
MULTILAYER INTERCONNECTS
MULTILEVEL
MULTIPROCESSOR SYSTEMS
NETWORK
NONLINEAR DEVICE MODEL
OHMIC CONTACTS
ON-BOARD TEST
OPTICAL INTERCONNECT
OXIDE ISOLATION
OXIDE
P-N JUNCTIONS
PARALLEL
PARAMETER EXTRACTION
PARAMETER
PARTICULATES
PARTITIONING
PATTERN RECOGNITION
PLA
PLACEMENT
PLASMA ETCH
PLASMA-ENHANCED
POLYCIDES
POLYIMIDE
POLYSILICON
POLYSILICON PROCESS EVALUATION
PROCESS INTEGRATION
PROCESS MODEL
PROCESS/DEVICE CHARACTERIZATION
PROCESSORS
PROGRAMMABLE DIGITAL SIGNAL
QUANTUM DEVICE
RADIATION
RECRYSTALLIZATION
REFRACTORY METALS
REGISTER TRANSFER
RELAXATION
RIBE
RIE
ROBOTICS
ROUTING
RTA OR RTP
SCHEDULING
SCHOTTKY GATE
SELF-TESTING
SEM
SEMICONDUCTOR
SENSORS
SHALLOW JUNCTION
SIGNAL PROCESSING
SILICIDE
SILICON COMPILATION
SIMULATION
SINGLE CRYSTAL
SOFT FAILURE
SOFTWARE ARCHITECTURE
SOFTWARE PORTABILITY
SOFTWARE RELIABILITY
SOI
SPEED-INDEPENDENT
SPUTTERING
STANDARD CELLS
STATISTICAL ANALYSIS
STATISTICAL PROCESS CHARACTERIZATION
STOCHASTIC PROCESS
STRESS
SUPERLATTICE SUBMICRON
SURFACE STATES
SWITCH-LEVEL SIMULATION
SYMBOLIC SIMULATION
SYSTEM PARAMETERS
SYSTEMS
SYSTOLIC ARRAYS
TEM
TEST AND RELIABILITY
TEST CHIP/STRUCTURE
TESTABILITY
THERMAL NITRIDATION
THERMAL SIMULATION
THIN OXIDE LAYERS
TIMING SIMULATION
TOPOLOGICAL DESIGN
TRANSITION METAL SILICIDES
TRANSMISSION LINES
TRENCHES
TUNGSTEN
TUNNELING
ULSI
ULTRACOMPUTER
VLSI
VPE
WAFER DIAGNOSTICS
WORKSTATION
WSI
X-RAY
YIELD MODELING
YIELD

February 12, 1988

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, Sept. 1, 1987 to November 31, 1987, SRC Project No. 84-07-051; "Analog CAD Methodology"

Introduction

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodology" from September 1, 1987 through November 31, 1987 or roughly the fall 1987 quarter. The objectives of this program are listed as follows:

1. Development of performance oriented analog CAD tools.
2. Development of accurate models, multilevel and mixed-mode simulators for and VLSI circuits.
3. Development of a means for circuit testability and fault diagnosis of analog integrated circuits.
4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective of reducing the design time for analog integrated circuits, increasing the chance of successful design and extending the design of analog integrated circuit to the systems designer.

Summary and Overview of Research Results

This research effort involves 8 PhD students and 1 Ms student. The students are Pjung Choi, Seong Hong, Harry Li, Juvena Loo, Alan Mantooth, John Parish, Mark Thrower, Kwang Yoon and Malsook Yu. Primary results for the fall include the completion of the AIDE2 Programmers Manual, further measurements of AIDE2 designed circuits, development of a modeling capability for GB, PSRR, and noise in switched capacitor filter simulation, the comparison of the table look-up model with BSIM and SPICE Level 2 models for a CMOS inverter, the evaluation of an 8-bit A/D converter designed by ADDAC, development of a program to generate circuit implementations of a general frequency independent two-port transfer function, and the development of functional macromodels for various nonlinear analog circuits and systems. The major accomplishment was to demonstrate that the table look-up model is more accurate and runs faster than other models presently used in simulation.

Report Organization

Each of the individuals working on this research program during the Fall 1987 quarter have written a brief summary of their efforts. These summaries follow this page. The research topic and student are listed as follows:

Mixed Mode Macromodeling of Nonlinear Analog Circuits & Systems	Pyung Choi
Cell Compiler and AIDE2 Research Activities	Seong Hong
ADDAC: An A/D and D/A Silicon Compiler	Harry Li
Automated Analog Integrated Circuit Design	Juvena Loo
Mixed, Analog-Digital Simulation	Alan Mantooth
Improvement of Existing Analog NMOS Multiplier	Mark Thrower
Precision Small Signal Model Development for Analog IC Design	Kwang Yoon
AIDE2	Malsook Yu

Budget Expenditures

The personnel supported by SRC during this quarter include Dr. Allen, Seong Hong, Alan Mantooth (SRC Fellow), John Parish, Kwang Yoon and Malsook Yu. The expenditures for this period are listed below:

Expenditure Category	Sept. 1987	October 1987	Nov. 1987	Totals
Personal Services	$7,360.00	$2,160.00	$4,913.00	$14,433.00
Fringe Benefits	$1,120.56	$0.00	$246.47	$1,367.53
Materials & Supplies	$176.66	$0.00	$155.12	$355.53
Travel	$0.00	$0.00	$0.00	$0.00
Computer	-	-	-	-
Overhead	$5,194.33	$1,310.25	$3,002.61	$9,507.19
TOTALS	$13,851.55	$3,494.00	$8,317.20	$25,622.75

MIXED MODE MACROMODELING OF NONLINEAR ANALOG CIRCUITS & SYSTEMS

Pyung Choi

January 8, 1988

Accomplishments

The object of my research is to develop a macromodel for an analog phase locked loop (PLL) that will predict dynamic loop behavior. During the fall quarter in 1987, a functional Voltage Controlled Oscillator (VCO) and Phase Detector (PD) macromodels were developed using several mini models such as a multiplier, integrator, limiter, triangular to sine wave converter, sine to square wave converter, and schmitt trigger. These macromodels can handle the linear and nonlinear characteristics of both actual VCO and PD. The basic idea of VCO modelling was a capacitor charge and discharge. The charging and discharging rates of capacitor depend upon the input DC voltage level. The multiplier model is a basic part of PD macromodel.

Plans

In the Winter quarter in 1988, SPICE simulation data of the macromodel for the PD and VCO will be compared with actual open loop device (LM565) experimental data such as the PD conversion gain and the VCO free running frequency. If the error is more than 1%, the macromodels will be modified to an error within 1%. All parts of the PLL will be connected to form closed loop system. Determine and compare performance of actual and macromodel PLL under unlocked, transition, and locked conditions.

Miscellaneous

Several papers that are concerned with digital-IC models such as NAND, Flip-Flop, Monostable Multivibrator, and Shift Register were surveyed. However these models were not applicable to SPICE program since FORTRAN subprogram was used for the description of some circuit elements of the macromodel. Based on the digital-IC models published, develop new digital-IC models for SPICE program and mixed mode simulator during the Winter quarter.

CELL COMPILER AND AIDE2 RESEARCH ACTIVITIES

Seong K. Hong

Quarterly Report for Fall 1987

Research Activities

The primary activity during the fall quarter has been developing the cell compiler for the AIDE2 program for the automated component design by using the procedural component generation technique. The basic component design starts with calling technology files for the generators to be compiled. Each technology file defines all technology-specific information for a given fabrication process, including physical layers, and design rules that specify minimum spacings and widths. Also, it is capable of generating any cell layout and all desirable databases from circuit description with the some control of choosing different technology and transistor size. It starts with constructing the transistors rather than polygons. Design rule independence can be achieved by expressing the position of the geometry in terms of foundry dependent design rules. That is, the required spacing and width will be determined by using the general notation instead of the specific number. Each transistor also generates relative position arrays which can be used by a module generator for size and aspect ratio estimates without actually calculating the geometry. For the convenience of estimating of the aspect ratio, transistors can be paralleled for the case of large W/L ratios.

The secondary activity has been developing the noise model for the opamp in AIDE2 program. To model the effects on the output noise of the opamp the noise can be considered as two parts: flat noise and flicker noise. To generate the flicker noise, a device model in figure 1 is used. The device is diode with biasing to dc current source, Isrc. The flat band noise can be modeled as white noise sources by using the resistors in SPICE. To model the flat-band noise, the resistor value is selected to match the measured input referred flat-band noise. In figure 1, the resistor Rn and the diode Df generate the white and flat band noise on the output of the opamp. Figure 2,3 shows the measured and simulated results for the noise of opamp.

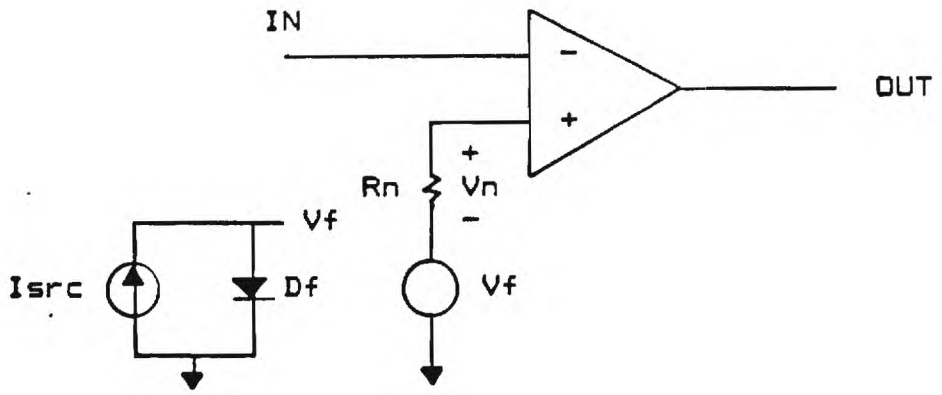


Figure 1. complete opamp noise model

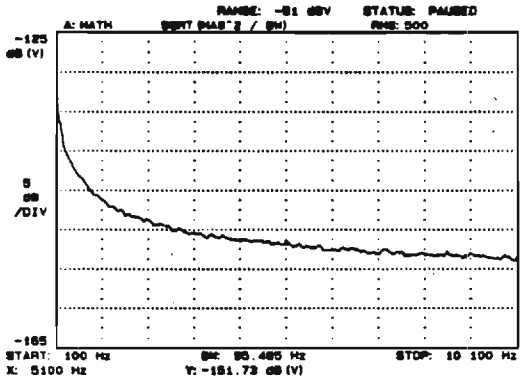


Figure 2. measured noise of opamp

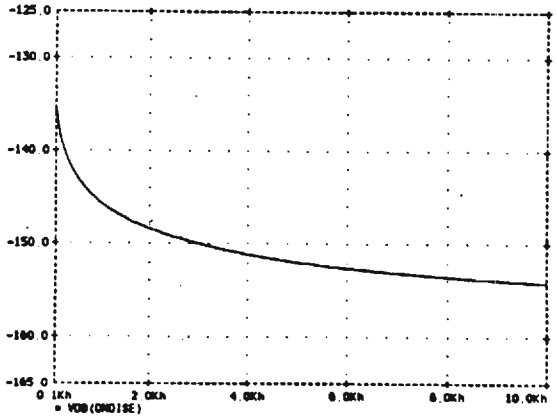


Figure 3. noise macromodel of opamp

ADDAC: An A/D and D/A Silicon Compiler

Harry W. Li

Fall 1987

I. Objectives

The goal of the fall quarter was to test and evaluate the latest fabrication of the successive approximation A/D converter generated by ADDAC. ADDAC is a high level application of the analog CAD tool, AIDE2. The building blocks which make up the converter are: the comparator block, sar_A and sar_B which compose the successive approximation register, a capacitor array, and a switch array.

II. Results

There were five chips associated with this fabrication, however, only three were fabricated due to a limited amount of resources. These three were the sar_B and comparator test chips, and an eight bit A/D. The two test chips which were fabricated proved to be working correctly. However, the A/D was discovered to have a large amount of power supply current. The problem was caused by a software error which shifted the entire switch array down and over by 2 lambda. This in turn caused an overlap between the power busses and ground. Micro-surgery was performed using an acoustical cutting probe and the short circuit was eliminated at the cost of the one least significant bit of resolution. However, a fatal error was discovered as a result of the software problem. It seemed that two ports were connected via two polysilicon runs which were shorted together by the shift. This was incorrectable through microsurgery since the polysilicon was not the top layer. There was also a layout error in which two latches in the sar_A cell had no Vdd connection. Along with the previous mentioned problems were random processing errors, all of which were shorts between two parallel metal runs. These proved to the most frustrating to deal with because of the length of time it took to discover them and the uncertainty introduced by them. The software and the layout errors were corrected and the circuit was resubmitted to MOSIS for fabrication.

Simulation of the A/D continued to be a problem. It seems the version of the mixed mode simulator, SPLICE, was not the most up-to-date and had trouble dealing with the analog portions of the circuit. The working version of SPLICE was recently obtained from the University of Illinois and will be evaluated.

III. Plans

While the circuit is being fabricated, the focus of this research will return to simulation. IGSPICE has been made available and allows functional descriptions of digital circuits. This should facilitate any needs that the successive approximation A/D requires. It is also hoped that the mixed mode simulator, SABRE, will be accessible and evaluated using the A/D.

AUTOMATED DESIGN OF ANALOG INTEGRATED CIRCUITS

Juvena Loo

February 10, 1988

Accomplishments

The object of this research is to develop methods of designing analog integrated circuits using the computer. In order to develop background and expertise, two programs have been developed for the design of simple CMOS op amps. The first program, called AUTOAMP, designs a 7-transistor op amp given the typical input specifications of an unbuffered op amp. This program has been used to design op amps which were fabricated and compared favorably with the specifications originally entered into the program. The second program also designed a CMOS op amp but permitted the selection of one of four possible topologies. The input stage had two different topologies and the output stage had two different topologies. The program would pick the structure that would best meet the user-weighted input specifications. This program has been debugged and has been used to design op amps which have not yet been submitted for fabrication.

The third phase of this research is the development of a general program capable of designing an analog circuit without the definition of prior topologies. Degenerate circuit elements have been used to idealize the active devices to permit the development of topology generation rules to achieve a given two-port specification. At the present, the two port specification is essentially the gain one of the four possible controlled sources along with the input resistance. Successful realizations have been made using this program. Fig. 1 shows the generation pattern that results from this program. When 4 resistors and four active devices are permitted, the program generated 38 possible realizations.

Plans

The plans for the Winter 1988 quarter are to develop an algorithm which simplifies the topology generation of the degenerate circuit element realizations. The next step will be to develop the algorithm which converts the generic degenerate circuit element realization into a practical implementation for a given technology. For example, Fig. 2a shows the degenerate circuit element realization corresponding to the circled realization of Fig. 1. Fig. 2b shows a BJT realization of Fig. 2a. Future plans call for extending the realization to a general n-node circuit and to include reactive as well as resistance elements.

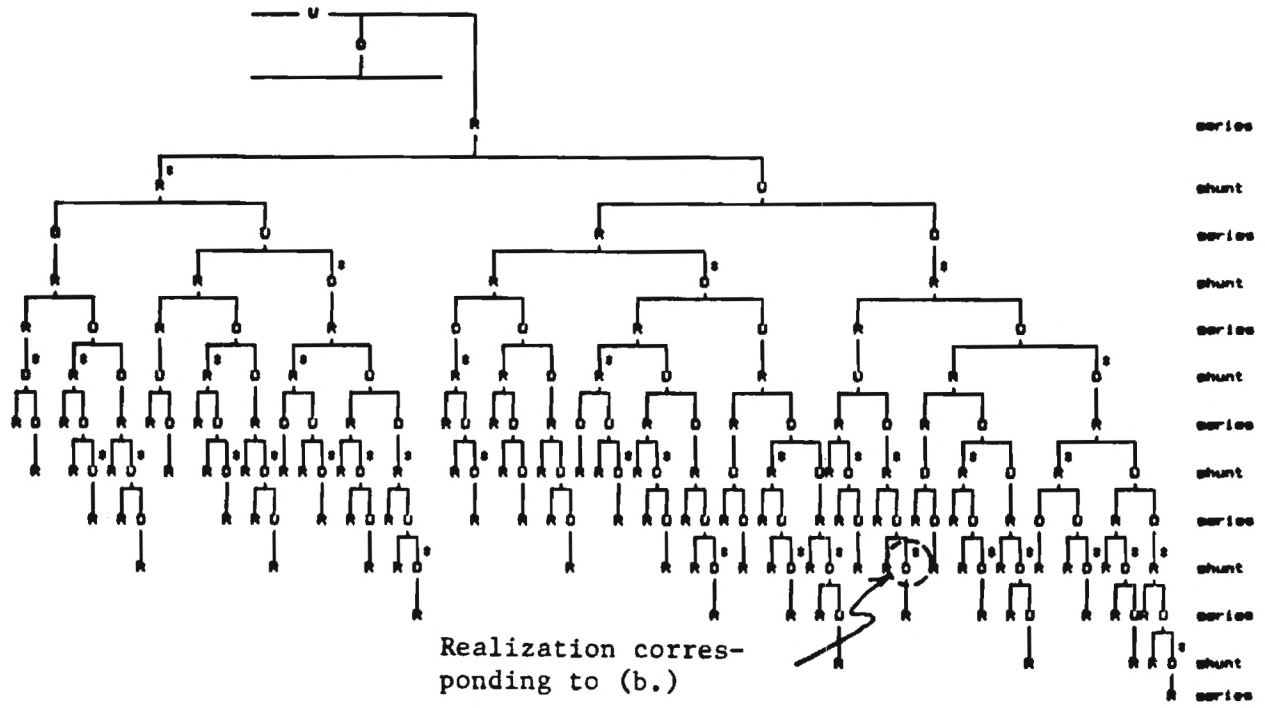
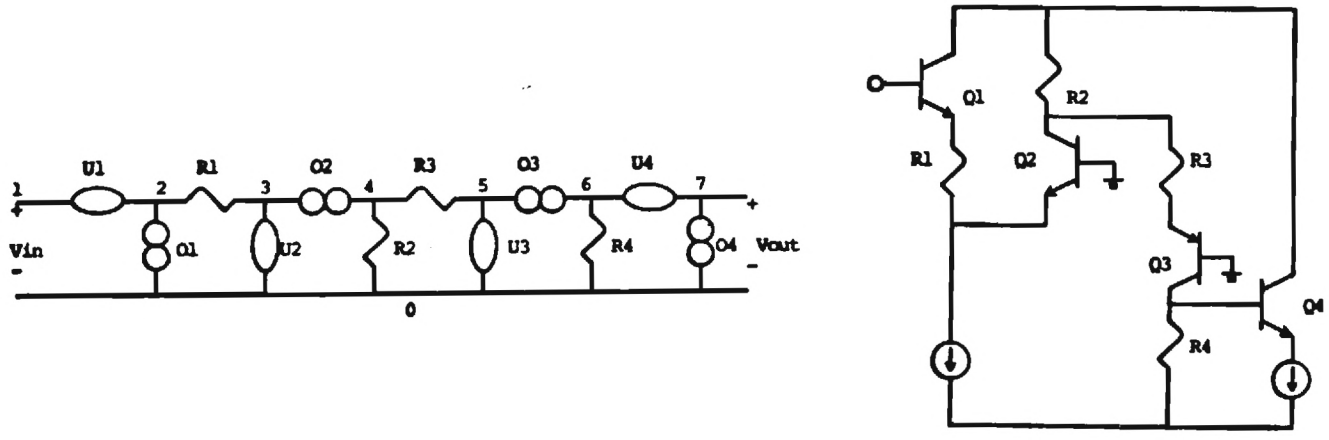


Fig. 1 - Example of degenerate circuit element realizations generated.



(a.) (b.)

Fig. 2 - (a.) Degenerate circuit element realization for circled case in Fig. 1. (b.) BJT realization of Fig. 2a.

Mixed Analog-Digital Simulation

H. Alan Mantooth

January 8, 1988

Accomplishments

The primary goal of the fall quarter was to identify viable areas of PhD research regarding mixed analog-digital simulation and to begin defining a specific related problem to be investigated at Georgia Tech which is of interest to SRC and its member companies. Several ideas have emerged as potential topics for research. Many of these are discussed in a report submitted to SRC in October. Some of these ideas are compatible with the expertise at Georgia Tech. As such, these are the ideas the will be pursued initially. These ideas address issues specifically brought forth by SRC member companies during visits in August and September.

Plans

The initial direction that will be taken deals with modeling. Modeling issues were mentioned many times during discussions with people from industry. A three to six month investigation into the possibility of automatically generating functional/behavioral models from SPICE for use in a higher level simulator will be performed. The simulator to be used for higher level simulation is Sierra Semiconductor's MIXsim. Investigations and evaluations of IGSPICE and SABER will be performed as well.

Publications

A report was submitted to SRC summarizing visits to the following list of companies.

Hayes Microcomputer Products	Aug. 1	Atlanta, GA
Rockwell International	Aug. 10	Newport Beach, CA
Hughes Aircraft	Aug. 11	El Segundo, CA
Silicon Systems	Aug. 12	Tustin, CA
Hewlett-Packard	Sept. 1	Santa Clara, CA
National Semiconductor	Sept. 2	Santa Clara, CA
GE Intersil	Sept. 3	Cupertino, CA
AT&T Bell Labs	Sept. 14	Murray Hill, NJ
General Electric	Sept. 17	Schenectady, NY
Analog Devices Semiconductor	Sept. 18	Wilmington, MA
Texas Instruments	Sept. 21	Dallas, TX

IMPROVEMENT OF EXISTING ANALOG NMOS MULTIPLIERS

MARK THROWER

JANUARY, 1988

I. OBJECTIVES

The goal of fall quarter was to redesign and layout an NMOS analog multiplier based upon the quarter square algebraic identity. Improvements in bandwidth were expected to be achieved through the use of cascode stages and a decrease in THD was expected to be achieved through level shifting and bias redesign around critical transistors.

II. RESULTS

The multiplier was designed using a combination of SLICE and human intuition. DC sweeps on SLICE reveal a theoretically successful multiplier with a gain constant of 0.1 and an input range of approximately 3 volts differential on either input. A viable layout was realized on the CALMA system in the Microelectronic Research Center.

III. PLANS

After an intense error check on the layout, the multiplier will be sent to Harris to be fabricated on the SSIV-A process. During the fabrication research activities will include an examination of AC and noise performance of the multiplier on SLICE as well as an examination of an existing state of the art multiplier with a 60 Mhz bandwidth manufactured by Analog Devices.

SRC Quarterly report on fall 1987

Precision small signal model development for analog IC design

Kwang S. Yoon

January 8, 1988

1. Objectives:

To develop models and model methodology which result in the computer efficient, accurate analog small signal models for short-channel MOSFETs, including the submicron devices.

2. Accomplishments:

The table look-up model has been developed to model both the large signal and the frequency independent small signal characteristics of MOSFET devices. This model has been used to benchmark MOS n-channel and p-channel devices from long-channel to short-channel devices. Table I shows that the table look-up model is at least an order of magnitude more accurate than BSIM and SPICE MOS level 2 models and is also faster than these two models. The W/L ratio used for n-channel and p-channel devices are 4.8mm/1.6mm and 1.6mm/1.6mm, respectively. The CMOS push-pull inverter with short-channel devices, which is shown in Fig. 1, has been used to benchmark the table look-up model. Comparisons were made between measured and simulated data from three models for the dc transfer curve shown in Fig. 2(a) and the voltage gain of the inverter shown in Fig. 2(b).

3. Plans:

The benchmark of table look-up model will be achieved for an operational amplifier with the minimum feature size of 1.6mm which was designed using CMOS bulk 1.25mm single poly and double metal n-well process. The intrinsic capacitances will be measured and modeled with the same table look-up approach.

TABLE I

	Accuracy (RMS % error)		cpu time (second)	
	NMOS	PMOS	NMOS	PMOS
BSIM	22.19	33.24	5.37	5.43
MOS 2	109.04	80.16	5.53	5.58
T.L.U.*	0.8	2.36	3.18	3.32

* Table look-up model is abbreviated by T.L.U.

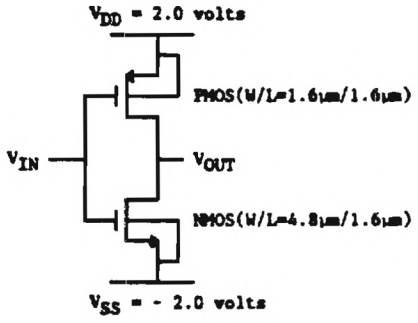
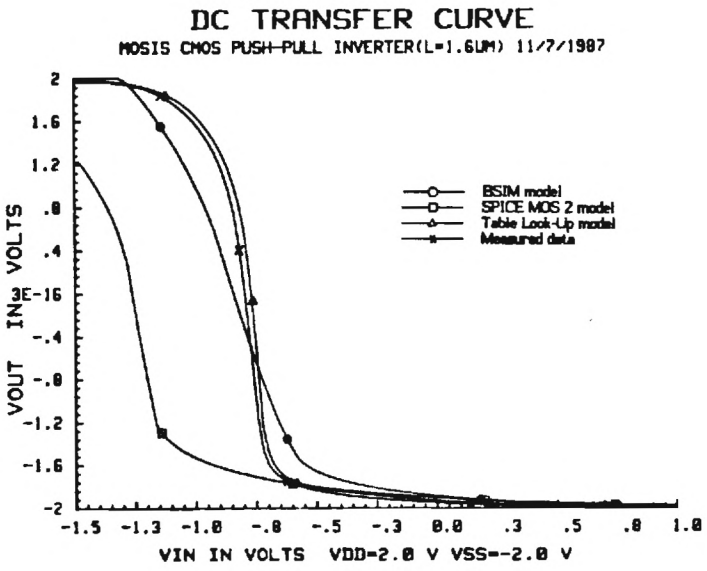
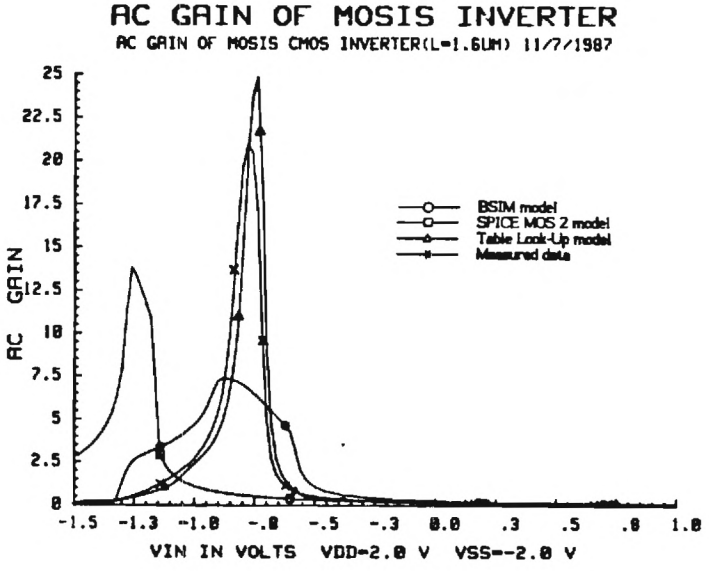


Fig. 1. The circuit schematic of a CMOS push-pull inverter with the minimum feature size of 1.6 micron.



(a)



(b)

Fig. 2. Comparison between measured and simulated data from three models for (a) the dc transfer curve and (b) the voltage gain of the CMOS push-pull inverter.

ANALOG INTEGRATED CIRCUIT DESIGN 2

MALSOOK YU

FALL, 1987

Accomplishments

My main goal was to write the Programmers Manual for the AIDE2 program and to identify the performance of limitations cause by CAD tools.
These were accomplished by :

1. Completed the AIDE2 Programmers Manual.
2. Measured the frequency response of three identical, third-order, low-pass filters which designed by AIDE2 with different aspect ratios.
3. Extracted the routing between parts of the various cells and between the V_{DD}, V_{SS}, and ground pad to each op amp.

Plans

My main goal is to measure the noise, PSRR, DC offset, voltage transfer function and power dissipation of those three filters and to write a SRC Report on "Influence of CAD Techniques on AIDE2 Designed Analog Circuits"

Publication

AIDE2.1 Programmer's Manual, December 15, 1987

E-21-636

SEMICONDUCTOR RESEARCH CORPORATION

COOPERATIVE
RESEARCH

29 January 1988

SRC Principal Investigators and Contract Administrators:

As we are at the beginning of the new year, it seems an appropriate time to remind you about the reporting requirements connected with your SRC contract. As you know, your contractual obligations include submitting Quarterly and Annual Reports on the progress of your research. You are also required to send the SRC copies of all papers, verbal presentations, or other disseminations of information prior to the date of first public disclosure. Plainly stated, any material resulting from your SRC-sponsored research must be sent to the SRC in written form before it is sent anywhere else. If you have any questions about these requirements please speak with your Contract Monitor at the SRC offices.

Each research connected document (Quarterly Report, Annual Report, thesis, journal preprint, presentation, etc.) must be accompanied by a completed SRC Report/ Publication Submission Form when you submit it to the SRC. Enclosed with this letter is a supply of the newly revised forms; although it may look a lot like the old one, there are small but important changes in it.

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Schlumberger Professor

Name and Address of Organization

School of Electrical Engineering

Georgia Institute of Technology

Atlanta, GA 30332

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ABSTRACT OF CONTENTS OF THIS SUBMISSION (must be in the space below or on a separate sheet of paper attached to this form)

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodlogy" from Dec. 1, 1987 through Feb. 29, 1988. If involves the research progress of 7 PhD students and 1 MS student. Primary results for the winter include the simulation of a phase locked loop on SPICE using macromodels, a generalized macromodel approach to creating a functional level simulation model for an arbitrary piecewise linear characteristic, the use of DC sensitivity capability of SPICE to identify circuit dependence upon the layout, simulation by IGSPICE of a 4-bit successive approximation AD converter, the improved design of a 4-quadrant NMOS analog multiplier, and the measurement of three identical AIDE2 designed circuits using a different layout. The major accomplishment was the application of the table look-up model to simulate the voltage transfer curve, ac gain, and ac output resistance of an op amp with 1 micron channel lengths. The results show that the table look-up model is an order of magnitude more accurate than BSIM and requires less CPU time.

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SCHOOL OF ELECTRICAL ENGINEERING
ATLANTA, GEORGIA 30332

TELEPHONE: (404) 894-6251

April 29, 1988

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, Dec. 1, 1987 to February 29, 1988, SRC Project No. 84-07-051; "Analog CAD Methodology"

Introduction

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodology" from December 1, 1987 through February 29, 1987 or roughly the winter 1988 quarter. The objectives of this program are listed as follows:

1. Development of performance oriented analog CAD tools.

2. Development of accurate models, multilevel and mixed-mode simulators for and VLSI circuits.

3. Development of a means for circuit testability and fault diagnosis of analog integrated circuits.

4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective of reducing the design time for analog integrated circuits, increasing the chance of successful design and extending the design of analog integrated circuit to the systems designer.

Summary and Overview of Research Results

This research effort involves 7 PhD students and 1 Ms student. The students are Pjung Choi, Seong Hong, Harry Li, Alan Mantooth, Mark Thrower, Kwang Yoon, Anna Yan, and Malsook Yu. Primary results for the winter include the simulation of a phase locked loop on SPICE using macromodels, a generalized macromodel approach to creating a functional level simulation model for an arbitrary piecewise linear characteristic, the use of DC sensitivity capability of SPICE to identify circuit dependence upon the layout, simulation by IGSPICE of a 4-bit successive approximation AD converter, the improved design of a 4-quadrant NMOS analog multiplier, and the measurement of three identical AIDE2 designed circuits using a different layout. The major accomplishment was the application of the table look-up model to simulate the voltage transfer curve, ac gain, and ac output resistance of an op amp with 1 micron channel lengths. The results show that the table look-up model is an order of magnitude more than BSIM and requires less CPU time.

Report Organization

Each of the individuals working on this research program during the Winter 1988 quarter have written a brief summary of their efforts. These summaries follow this page. The research topic and student are listed as follows:

Mixed Mode Macromodeling of Nonlinear Analog/Digital Circuits & Systems	Pyung Choi
Cell Compiler and AIDE2 Research Activities	Seong Hong
ADDAC: An A/D and D/A Silicon Compiler	Harry Li
Mixed, Analog-Digital Simulation	Alan Mantooth
Improvement of Existing Analog NMOS Multiplier	Mark Thrower
Precision Small Signal Model Development for Analog IC Design	Kwang Yoon
8-Bit A/D Converter Simulation	Anna Yan
AIDE2	Malsook Yu

Budget Expenditures

The personnel supported by SRC during this quarter include Dr. Allen, Seong Hong, Alan Mantooth (SRC Fellow), John Parish, Kwang Yoon and Malsook Yu. The expenditures for this period are listed below:

Expenditure Category	Dec. 1987	January 1988	Feb. 1988	Totals
Personal Services	$9,173.00	$2,880.00	$2,880.00	$14,933.00
Fringe Benefits	$246.47	$0.00	$0.00	$246.47
Materials & Supplies	$153.95	$31.00	$650.92	$835.87
Travel	$0.00	$0.00	$0.00	$0.00
Computer	-	-	-	-
Overhead	$5,744.05	$1,746.65	$2,118.55	$9,609.25
TOTALS	$15,317.47	$4,657.60	$5,649.47	$25,624.59

MIXED MODE MACROMODELING OF NONLINEAR ANALOG/DIGITAL CIRCUITS AND SYSTEMS

Pyung Choi
April 4,1988

Accomplishments

a. Analog Phase Locked Loop Macromodel

A draft functional simulation model for analog phase locked loop (APLL) is developed. Functional behavior of the APLL macromodel is well matched to theoretical expectations. However SPICE simulation results of the APLL macromodel have suffered large CPU time and accuracy problems with respect to measured data of NE 565F.

b. Modeling Techniques

A generalized macromodel approach to create functional level simulation models from arbitrary single valued piecewise linear functions has been developed and programmed using BASIC. A simple coordinate description of a piecewise linear function is used to automatically generate macromodels as subcircuit forms for direct inclusion into SPICE family circuit simulators.

Plans

a. Modify the draft APLL model to improve the accuracy and the simulation time in SPICE.

b. Develop a model for a 1200 baud Hayes modem digital phase locked loop (DPLL) using SABER.

c. Convert SPICE functional models, that are already developed, into SABER templates as behavior or functional types.

d. Improve the generalized macromodel approach to automatically create functional simulation models from behavior description (transfer functions) for SPICE families.

Publications

a. Submitted summary and abstract, which title is "A Generalized SPICE Macromodel for Piecewise Linear Circuits and Systems", to 31st Midwest Symposium on Circuits and Systems.

CELL COMPILER AND AIDE2 RESEARCH ACTIVITIES

Seong K. Hong
Quarterly Report for Winter 1988 quarter

Research Activities

The primary activity during the this quarter has been developing the cell compiler for the automated component design methodology. The objective of this research is to develop a software program which can take a SPICE input file and automatically create a layout which has been optimized according to a user specified performance.

First of all, we investigated how to generate the cell with the enhanced performance. The circuit performance is very dependent on the parasitic elements on the interconnections between the devices. We analyzed the circuit performance with respect to the layout parasitics by using the sensitivity analysis in SPICE program. As shown in figure 1 and 2 circuit the performance with the consideration on the parasitics deviated from the performance without the parasitics. Specifically, the parasitics on the sensitive nodes has more influence on the circuit performance rather than those on the nonsensitive nodes. We have concluded that the circuit should be laid out with shorter interconnects on the sensitive nodes, if possible.

Before the sensitivity analysis, the original circuit structure given by user should will be modified in order to perform the sensitivity analysis. The interconnections between components will be replaced by resistor-capacitor equivalent of the parasitics. The sensitivity of the specific circuit performance will then be calculated with respect to the parasitic resistors and capacitors. Figure 3 shows a simple example of the transformation from an inverter without parasitics to that with parasitics. Also, the program can automatically generate the input file for the sensitivity analysis after reordering the netlist with embedded parasitics. We are now trying to develop the capability to make an ac sensitivity analysis which is not found in simulation programs such as SPICE.

Publications and Presentations

On Jan. 14, 1988, a paper titled "BUILT IN TESTABILITY FOR AUTOMATICALLY GENERATED ANALOG CIRCUITS" was presented at the ATE & Instrumentation Conference at Anaheim, CA.

On Feb. 5, 1988, we had a presentation on the visit by GE schenectady concerning on the cell compiler.

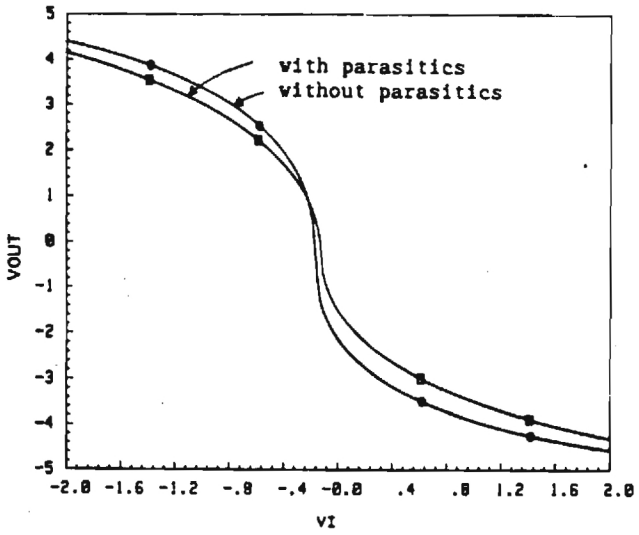

Figure 1. parasitic effect on inverter

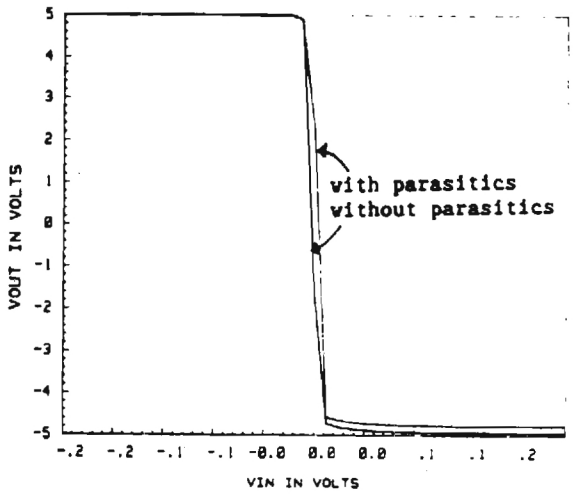

Figure 2. parasitic effect on opamp

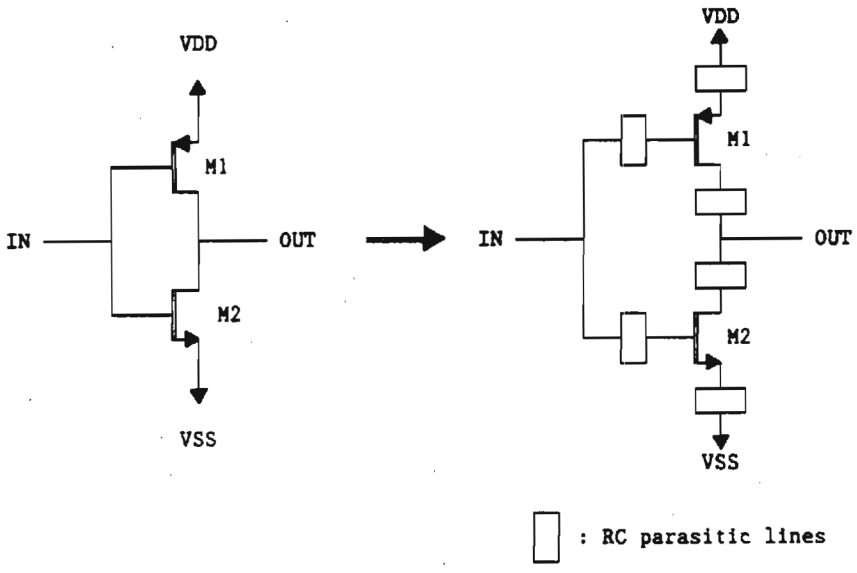

Figure 3. Inverter without / with parasitic elements

ADDAC: An A/D and D/A Silicon Compiler

Harry W. Li
Winter 1987

I. Objectives

The objective is the simulation of an A/D converter using IG_SPICE. IG_SPICE is a SPICE-like simulator which allows functional level descriptions of digital circuits and also allows the implementation of external Fortran coded models.

II. Results

The strategy for simulation of the A/D was to simulate at the highest level possible and to only implement a four-bit A/D. The comparator was initially described with a macro-model and eventually replaced with its transistor level equivalent. Sections of the converter were simulated individually in order to localize any convergence problems. There were some DC convergence problems which were remedied with the .NODESET card and by adding delay to certain signals. Eventually, all the digital portions of the converter were successfully simulated. The simulation of the entire converter revealed several design errors. These included the following: 1) A RS flip-flop has an undefined state during power-up which charges up the capacitor array to an erroneous voltage. 2) Because this condition was unexpected there was no way for the capacitor array to discharge before the conversion began, hence, the result of the conversion was wrong. 3) The accuracy of the converter was limited by the fact that throughout the circuit many pass transistors were used which consisted of a single n or p type MOS device. A threshold drop occurs across each N pass transistor transmitting a logic one and across each P pass transistor transmitting a logic zero.

The first two errors were corrected in the simulation by delaying a signal which controls a toggle switch connecting the bottom side of the capacitor array from ground to the input voltage. This will allow time for another controlling signal to connect the top plate of the capacitor array to ground thereby shorting-out the capacitors. The third error was remedied by replacing each single device pass transistor with a CMOS transmission gate which does not require any threshold drop across it when transmitting either a zero or a one. Once these errors were corrected, the simulation ran successfully.

III. Plans

The plans for the next quarter will be to redesign the A/D. This will include ridding the circuit of the RS flip-flop, delaying the signal responsible for discharging the capacitors, and replacing all pass transistors with transmission gates. The circuit will be resimulated and the layout extracted in order to verify the changes. Also, the fabrication from the previous MOSIS submission has been returned and will be evaluated to verify these design errors.

Mixed Analog-Digital Simulation

H. Alan Mantooth
April 18, 1988

Accomplishments

The goals of the winter quarter were twofold. The first goal was to investigate the possibility of automatically generating behavioral models from SPICE to enhance multilevel analog and mixed analog-digital simulation. The second goal was to evaluate the multilevel analog capabilities of IGSPICE and SABER. Investigations into automatic behavioral model generation were begun. The models are determined from circuit level simulations and/or data sheet specifications. At present, models are generated in the C programming language, not for a specific simulation tool. The multilevel analog and mixed analog-digital circuit and system capabilities of IGSPICE and SABER were under investigation. A week-long SABER training course was attended in Beaverton, Oregon. The circuit used for simulation is an 8-bit successive approximation A/D converter. It was determined that IGSPICE was severely limited in its behavioral level modeling capabilities. SABER is under further investigation.

Plans

Further investigation into automatic behavioral model generation is necessary. Intentions are to apply these modeling techniques to the SABER simulator for evaluation. Investigations of IGSPICE and SABER will continue. The two-month-long Ph.D. Qualifying Examination will be taken from mid-March to mid-May.

IMPROVEMENTS OF AN EXISTING ANALOG NMOS MULTIPLIER

Mark Thrower
April 1, 1988

Accomplishments

The four quadrant NMOS multiplier was redesigned to include PMOS transistors to allow a single ended voltage output. A buffer stage was added to allow the multiplier to realistically drive a real world capacitive load. Resistors were completely eliminated from the design. The cascode configurations were discovered to be useless in this design and were removed.

The new multiplier has 40 transistors, a THD of less than 1% for control voltages inside 3 volts DC and sinusoids inside 3 volts peak to peak, and a bandwidth of 3 Mhz into a 20 pf load. The output is single ended but possesses a -1.5 volt DC offset due to the output buffer stage.

Plans

The multiplier is to be fabricated this Spring and Summer. Research activities involve putting together tapes containing the multiplier as well as 30 or so other circuits to be fabricated in the Harris SSIV-A process. After the tapes are sent, research will shift towards Gallium Arsenide and the possibility of a Gallium Arsenide multiplier.

PRECISION SMALL SIGNAL MODEL DEVELOPMENT FOR ANALOG IC DESIGN

Kwang S. Yoon
April 4, 1988

1. Objectives:

To develop models and model methodology which result in the computer efficient, accurate analog small signal models for short-channel MOSFETs, including the submicron devices.

2. Accomplishments:

Since the device characteristics are exposed to the process variations, it was necessary to determine the statistical accuracy of the table look-up dc and ac models. In order to obtain this accuracy, one short-channel device (NMOS W/L=4.2um/1.0um) with the typical device characteristics has been extracted to create a table array and BSIM model parameters. Twenty transistors with the same geometry have been measured on the different dies, so that rms errors have been calculated between the measured and simulated data from both table look-up and BSIM model. Fig. 1 shows that the statistical dc model accuracy of both table look-up and BSIM is equivalent to within 5% and that the table look-up ac model, especially output conductance and substrate transconductance is more accurate than BSIM ac model. When device scalings and process variations are taken into account, the statistical accuracy of table look-up dc and ac model is found to be approximately within 10%.

The benchmark of the table look-up model has been achieved, using the operational amplifier with the minimum feature size of 1.0um. Table 1 illustrates that the accuracy of table look-up model is within 10% to predict the open loop gain of the operational amplifier. Table look-up, BSIM, and spice MOS 2 model parameters have been extracted to simulate the operational amplifier. The accuracy and computational efficiency of each model are shown in Table 2.

3. Plans:

The instrinsic capacitances will be modeled and benchmark of capacitance modeling will be achieved in terms of the device and circuit level

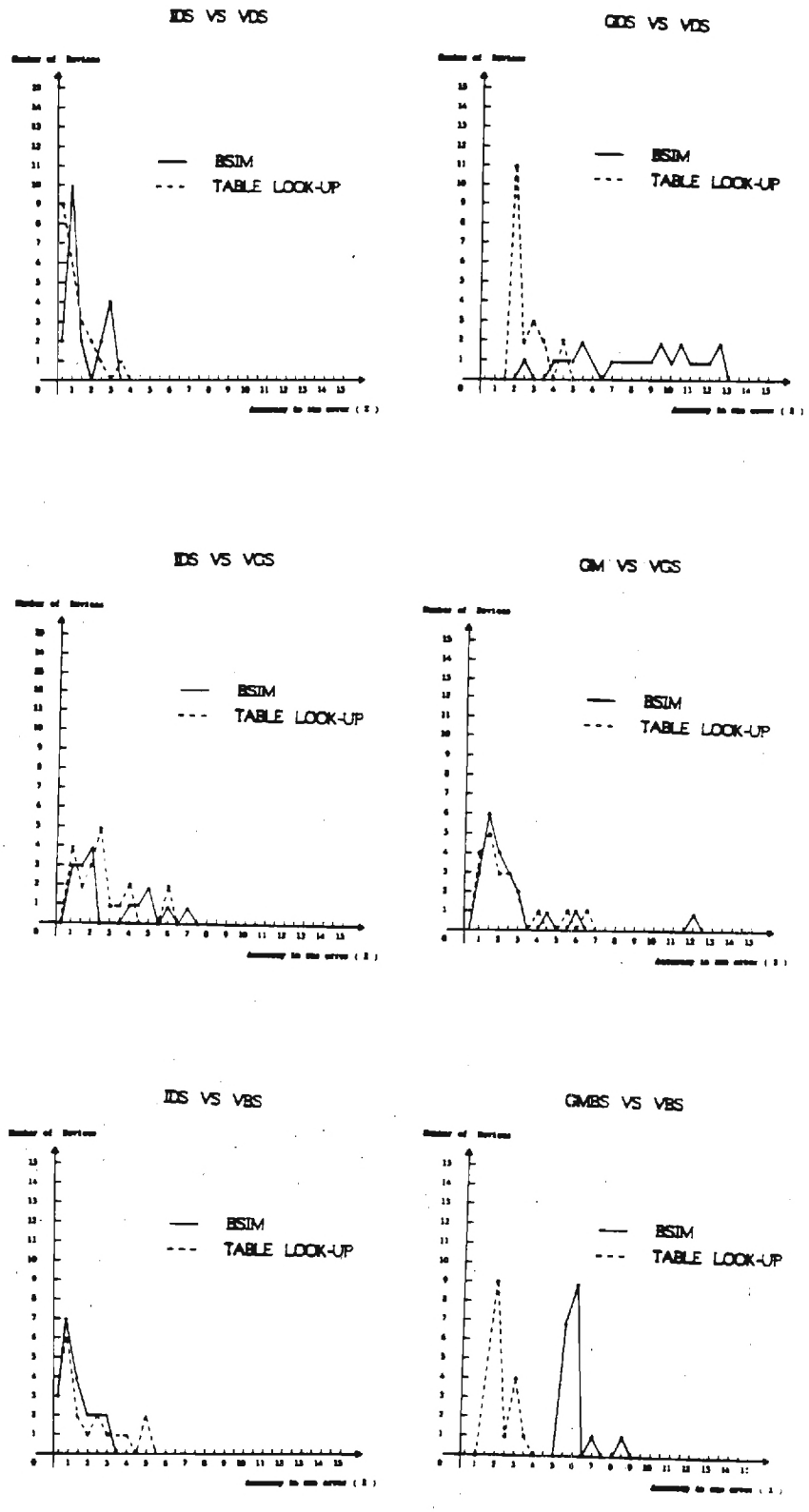

Fig. 1. Statistical accuracy of table look-up and BSIM model (dc and ac) for NMOS W/L=4.2um/1.0um device.

Table 1. The comparisons of the open loop gain of the 16 opamps between the measured and simulated data from table look-up model

Die No.	A_{VS}(dB)	A_{VS}	A_{VM}(dB)	A_{VM}	rms error (%)
A21	49.28	291.2	49.52	299.2	2.68
A31	49.59	301.9	49.55	300.3	0.54
A41	48.89	278.3	49.88	311.9	10.77
A51	49.17	287.5	49.41	295.5	2.69
A61	48.80	275.4	48.96	280.5	1.83
A22	48.91	279.0	49.70	305.5	8.67
A32	48.51	266.3	49.35	293.4	9.24
A42	49.80	311.4	49.35	293.4	6.12
A52	49.17	287.4	49.22	289.9	0.58
A23	49.90	312.7	49.62	302.7	3.31
A33	49.32	292.4	50.17	322.5	9.33
A43	48.78	274.8	49.20	288.4	4.72
A53	49.72	306.3	50.03	317.3	3.47
A63	49.68	298.0	49.60	302.0	1.32
A24	49.07	284.1	49.20	288.4	1.49
A54	50.28	326.6	49.33	292.8	8.15
Average	49.29	291.5	49.51	298.7	2.41

Table 2. The comparisons of table look-up, BSIM, and spice MOS2 model with respect to accuracy and computational efficiency.

Model	A_V	A_V(dB)	error (%)	cpu (seconds)
Table	291.2	49.28	2.68	14.65
BSIM	340.4	50.64	15.72	15.15
MOS2	180.3	45.12	39.75	17.25

8-BIT A/D CONVERTER SIMULATION

Anna Yan

April 4, 1988

Accomplishments

The goal of the winter quarter was to use IGSPICE to simulate the 8-bit A/D converter designed by ADDAC. Because of the simulation time, the 4-bit A/D converter was simulated instead of 8-bit A/D converter.

First, A/D converter was simulated part by part. Based on those parts, then, a 4-bit A/D converter with a functional macromodel for comparator and a 4-bit A/D converter with transistor-level model for comparator were successfully simulated. The results associated with these two different comparator models were consistant.

The main problem encountered were:

1. DC analysis was not convergent because of undefined votage values at some nodes in initial case;
2. Transient analysis was not able to be accomplished partly due to the same reason as 1. in transient analysis and partly due to the timing sequence problems resulted from ideal digital elements in original design;
3. Some unexpected simulation results came out because a few parts of the converter such as sar_b and transmission gates were designed incorrectly.

In order to complete the simulation and get the correct result some modifications were made:

1. "NODESET" was used to define some initial voltage values in DC analysis;
2. Time delay was added to the digital gates which might cause transient analysis not to be finished;
3. The circuit was modified as needed.

Plans

In the Spring quarter, the A/D converter will be redesigned and resimulated by using IGSPICE, then simulated by using SABER. The results will be compared.

PERFORMANCE CAPABILITIES OF AIDE2 DESIGNED CIRCUITS

Malsook Yu
Winter, 1988

Accomplishments

The main goal for the winter quarter was to identify the performance of limitations cause by CAD techniques. From the experimental results, the measurements of the frequency response of three identical, third-order, low-pass filters which designed by AIDE2 with different aspect ratios, some differences between three filters were observed. There were several approaches I followed in order to verify the differences by considering the differences in routing and placement. First, evaluated the performance of the AIDE2 designed circuits on the Harris fabrication. Second, extracted parasitics of three filters. Third, simulated the performance including the parasitics. Then, compared with the experimental results. Table 1 shows the average frequency response characteristics of three of each of the three different layouts. Table 2 shows the extracted results between V_{IN} and V_{OUT} to each op amp. Including these data, the performance had been simulated. However, the simulated results was not corresponded properly.

Plans

The main goal for the spring quarter is to evaluate and verify the methods to improve the simulation including ideal and nonideal aspects of the op amp or the switched capacitor circuit.

Frequency Response Characteristic	Simulated Data with finite Gain Bandwidth	Experimental Data		
		FILTER3N (R=100)	ELIPEX (R=50)	FIL3 (R=200)
Amplitude at 10 Hz (Hz)	-6.015	-7.071	-7.342	-7.187
Frequency of the peak (Hz)	35480	34145	31623	32434
Amplitude of the peak (dB)	-6.806	-3.966	-5.766	-5.121
Phase at the peak freq.	-115.5°	-138.0°	-124.8°	-133.7°
Frequency of notch (Hz)	100,000	95,075	85,770	117,262
Depth of the notch (dB)	-50.78	-55.42	-68.73	-65.21
Phase at the notch	-91.18°	10.59°	-146.36°	-119.49°

Table 1 - Average frequency response characteristics of three of each of the three different layouts (R=100 is square, R=50 is short and wide, and R=200 is tall and thin).

	FILTER3N (R = 100)		ELIPEX (R = 50)		FIL3 (R = 200)	
	LIB1-VIN	LIB3-VOUT	LIB1-VIN	LIB3-VOUT	LIB1-VIN	LIB3-VOUT
RESISTORS(ohms)	1714.95	1884.56	720.96	920.85	1589.81	1903.01
CAPACITORS(-17F)	5.792	6.535	3.578	6.043	4.918	5.406

Table 2 - Extracted parameters of three filters

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Phillip E. Allen
Schlumberger Professor

Name and Address of Organization

School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

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This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodology" conducted at Georgia Tech during the period of Mar. 1, 1988 through May 31, 1988. It involves 6 PhD students. The report is organized with a general summary followed by a one page description by each student on his/her research progress. The primary research activities described are (1) the precision modeling of devices by table look-up methods and (2) the use of macromodels to simulate the performance of complex analog circuits using SPICE. Other research activities described in report include the identification of constraints for an automated layout program including the use of DC and AC sensitivity capability of SPICE-PAC to identify circuit dependence upon the layout, simulation by IGSPICE and SABER of a 4-bit successive approximation AD converter, redesign of ADDAC program to eliminate errors, and the measurement and analysis of three identical AIDE2 designed circuits using a different layout to determine layout-dependent performance limitations.

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Name of Person Responsible (PI or Administrative Person)	Name and Address of Organization
Phillip E. Allen	School of Electrical Engineering Georgia Institute of Tech., Atlanta, GA 30332

REPORT TITLE
Quarterly Report - March 1988 through May 31, 1988

REPORT AUTHOR(S)
Phillip E. Allen

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[ ]	Publication: Name of Journal _____	_____
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Name(s) Phillip E. Allen

Title(s) Professor

Organization(s) Georgia Tech

Date Reviewed July 28, 1988

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[ ] Patent Application: US Serial No. & Filing date: _____

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July 28, 1988

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, March 1, 1988 to May 31, 1988, SRC Project No. 84-07-051; "Analog CAD Methodology"

Introduction

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analog CAD Methodology" from March 1, 1988 through May 31, 1988 or roughly the Spring 1988 quarter. The objectives of this program are listed as follows:

1. Development of performance oriented analog CAD tools.
2. Development of accurate models, multilevel and mixed-mode simulators for and VLSI circuits.
3. Development of a means for circuit testability and fault diagnosis of analog integrated circuits.
4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective of reducing the design time for analog integrated circuits, increasing the chance of successful design and extending the design of analog integrated circuit to the systems designer.

Summary and Overview of Research Results

This research effort involves 6 PhD students. The students are Pjung Choi, Seong Hong, Harry Li, Alan Mantooth, Kwang Yoon, and Anna Yan. The research activities in the precision analog device models using a table look-up approach and the use of macromodels for simulating complex analog circuits have reached a point of maturity and are showing excellent results. The table look-up model has been applied to complex analog circuits and gives results having an order of magnitude reduction in error and using less CPU time than the BSIM model. The approximate storage requirement for one transistor is 6KBytes.

The macromodeling research has been applied to the simulation of an analog phase locked loop (PLL) on SPICE. The dynamic performance of the analog PLL has been simulated using reasonable CPU times (20 minutes on a PC). A generalized macromodel approach to creating a functional level simulation model for an arbitrary piecewise linear characteristic has been developed and applied allowing the quick macromodeling of such characteristics. Behavioral

models have been developed for both analog and digital PLL's in order to simulate these circuits on the SABER simulator.

Other research activities described in this report include the identification of constraints for an automated layout program including the use of DC and AC sensitivity capability of SPICE-PAC to identify circuit dependence upon the layout, simulation by IGSPICE and SABER of a 4-bit successive approximation AD converter, redesign of ADDAC program to eliminate errors, and the measurement and analysis of three identical AIDE2 designed circuits using a different layout to determine layout-dependent performance.

Malsook Yu finished her MS degree and accepted a job at Silicon Systems in Tustin, CA.

Report Organization

Each of the individuals working on this research program during the Spring 1988 quarter have written a brief summary of their efforts. These summaries follow this page. The research topic and student are listed as follows:

Macromodeling for Complex Nonlinear Analog Circuits and Systems	Pyung Choi
Cell Compiler and AIDE2 Research Activities	Seong Hong
ADDAC: An A/D and D/A Silicon Compiler	Harry Li
Mixed, Analog-Digital Simulation	Alan Mantooth
Precision Small Signal Model Development for Analog IC Design	Kwang Yoon
8-Bit A/D Converter Simulation	Anna Yan

Budget Expenditures

The personnel supported by SRC during this quarter include Dr. Allen, Pyung Choi, Seong Hong, Alan Mantooth (SRC Fellow), and Kwang Yoon. Anna Yan who worked on SRC research was supported from the Schlumberger Chair funds. The SRC expenditures for this period are listed below:

Expenditure Category	March 1988	April 1988	May 1988	Totals
Personal Services	$2,880.00	$3,349.16	$2,880.00	$9,109.16
Fringe Benefits	$0.00	$40.35	$0.00	$40.35
Materials & Supplies	$2,043.59	$804.02	$487.38	$3,334.99
Travel	$0.00	$0.00	$717.02	$717.02
Computer	-	-	-	-
Overhead	$2,954.15	$2,516.12	$2,450.64	$7,920.91
TOTALS	$7,877.74	$6,709.65	$6,535.04	$21,122.43

MACROMODELING FOR COMPLEX NONLINEAR ANALOG CIRCUITS AND SYSTEMS

Pyung Choi
July 5, 1988

I. Objectives and Accomplishments

The primary goal of the Spring quarter 88 was to test and evaluate a functional level model of analog phase locked loop (APLL). PSpice was used to verify dynamic behavior of the APLL macromodel such as capture, tracking ranges, and pull-in time. The simulation results showed good performance of the APLL model. The lock procedure and pull-in time could be achieved from the step changing input which was within capture range. Out of capture range simulation, the output of loop filter was almost zero DC voltage so that output frequency of the APLL model remained in the free running frequency. The capture and tracking ranges could be obtained from the increasing (for low capture and high tracking frequency) and decreasing ramp inputs (for high capture and low tracking frequency). For the rapid changing ramp input, the APLL macromodel did not achieve the lock state.

The secondary objective was to develop a behavior level model for digital phase locked loop (DPLL) and to upgrade generalized modeling technique for continuous filtering functions. For the DPLL model, a voltage controlled oscillator (VCO) model has been developed and analyzed using SABER. The major portion of electrical parameters of actual VCO has been implemented into the behavior model. For modeling of continuous filtering function, a generalized technique has been developed. The modeling technique was derived from Mason's flow graph gain formula. It is applicable to design and simulation of linear part of complex nonlinear analog circuits and systems.

II. Plans

The plans for the next quarter are: (1) Modify the APLL macromodel to match the actual APLL device data such as NE 565F, (2) Develop digital phase locked loop behavior model using Saber, (3) Develop a generalized modeling technique for discrete transfer functions, and (4) Program for automatic generation of functional level models for behavior description of continuous transfer functions.

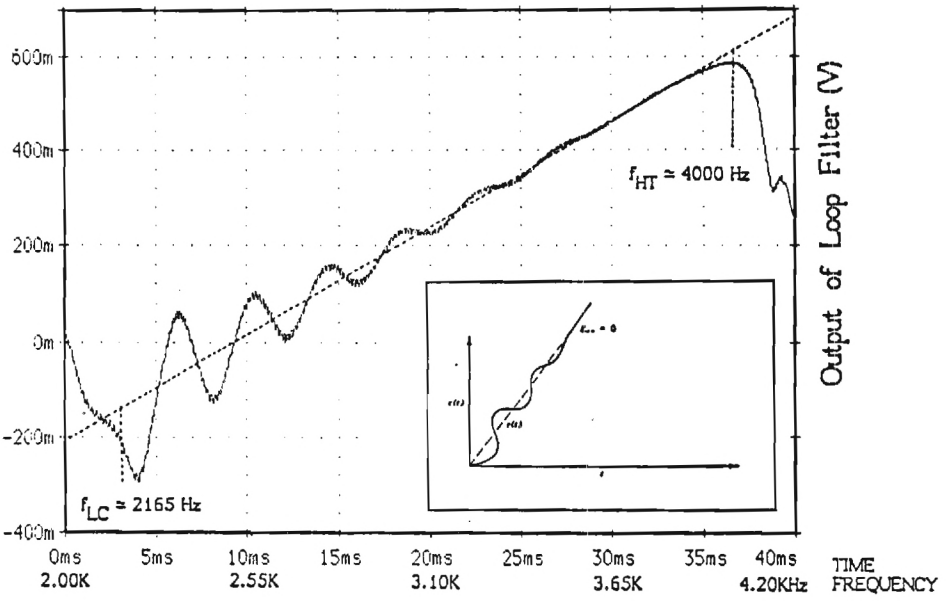


Fig.1 Output Voltage of Loop Filter for Ramp Input (Frequency Sweep Rate= 55 Hz/ms)

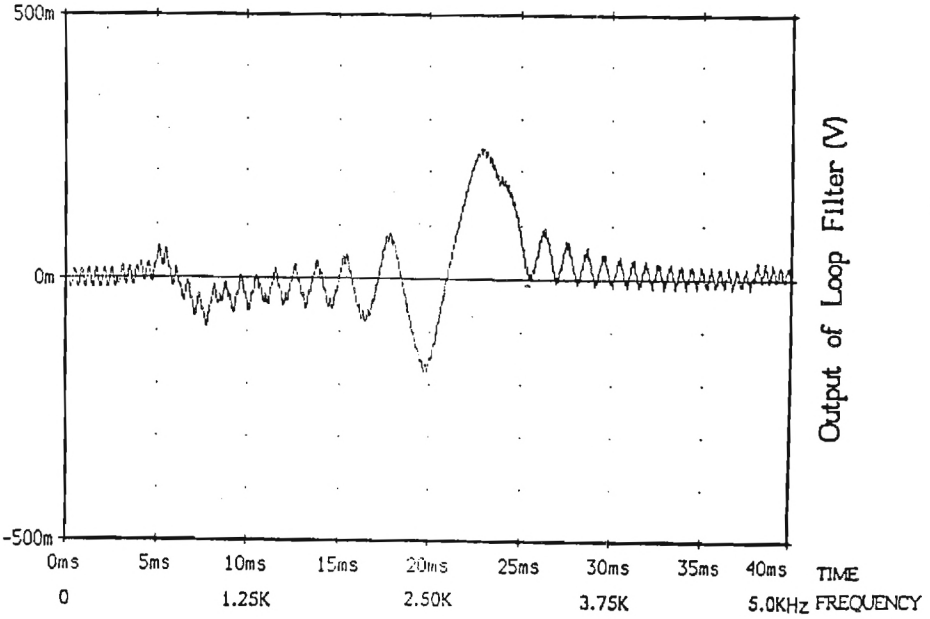


Fig.2 Output Voltage of Loop Filter for Ramp Input (Frequency Sweep Rate= 125 Hz/ms)

CELL COMPILER AND AIDE2 RESEARCH ACTIVITIES

Seong K. Hong
Quarterly Report for Spring 1988 Quarter

Objectives

1. **Cell Compiler** - to develop a software program which can take a SPICE input file and automatically create a layout which has been optimized according to a user specified performance.

2. **Performance of AIDE2 Designed Circuits** - to develop the tools and modeling technique which provide enhanced performance that approaches custom design circuits by comparing the performance of AIDE2 circuits with identical custom designed circuits.

Accomplishments

The primary activity has been developing the automated component design methodology. First of all, we analyzed the circuit performance with respect to the layout parasitics on the interconnections between the devices. From the result of the sensitivity analysis we concluded that layout interconnect must use the low resistance layer for: 1. any source connected to power supply. 2. any two sources connected together. 3. if the gates and sources are connected together. 4. any branch which carries large current. We are now using the above results in order to implement the rule based design technique on the cell compiler for the final layout. For the device generation design rule independence can be achieved by expressing the physical definition in terms of the design rules and parallel type (or snake type) of transistor can be used for the case of transistor which has the unreasonable width/length ratio. For the placement and routing strategy net tracing algorithm is now in development. The objective of component placement is to achieve the optimum user specified performance by maximizing the number of neighboring single-layer routing connections or selecting the lowest parasitic interconnection between two components.

The secondary activity has been implementing the several op amp models into the switched capacitor filter to compare the performance of AIDE2 designed circuits with the identical custom designed circuit. We used the HC5512A PCM receive filter fabricated from HARRIS corporation. Figure 1, 2, and 3 shows the comparison between the simulation data and two measured data (from AIDE2 designed circuit and HC5512A) for the frequency response, power supply rejection ratio, and noise, respectively.

Plans

1. Implementation of the net tracing algorithm for the placement and routing.
2. Development of ac sensitivity analysis capability by using the SPICE-PAC program.
3. Consideration on the recognition rules of various configuration such as diff_amp and cascode type.

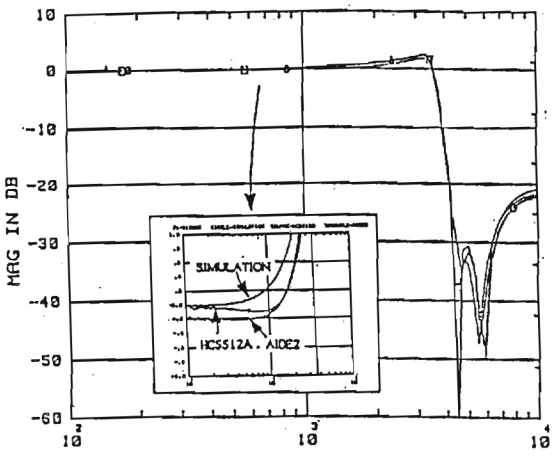


Figure 1. Frequency Response

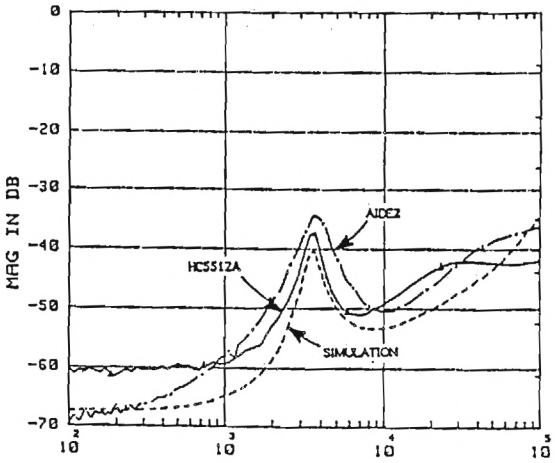


Figure 2. Power Supply Rejection Ratio

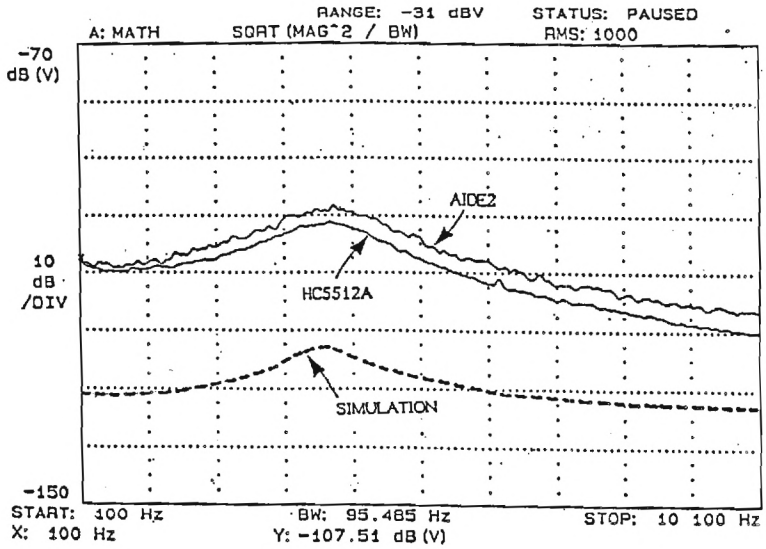


Figure 3. Noise

ADDAC: An A/D and D/A Silicon Compiler
SRC Quarterly Report
Harry W. Li
Spring 88

I. Objectives

The redesign and modification of the A/D converter used in ADDAC and the examination of the effects of automated layout on the performance of a third order low pass filter.

II. Results

The A/D converter was found to have several design errors. The following modifications were made:

1. Redesigned sar_B (one bit shift register) see fig. 1.
2. Modified sar_A (control logic) to eliminate timing problems.
3. Added transmission gates to capacitor array.
4. Created new switch array.

These changes were verified using IG_SPICE and the layout was verified using Magic. A ten bit A/D and a one bit test circuit was submitted to Harris Corporation.

Three identical third order low pass filter were laid out using three different aspect ratios (200 is tall and thin, 100 is square, 50 is short and wide). Three different chips were measured for each filter and the data examined. It was observed that below a clock frequency of 1MHz the filter response were identical. However, at 1 MHz, there were some differences between the filters and the simulated data. This was caused by several reasons:

1. The process dependencies caused wide variation in the data.
2. The parasitics due to routing and placement increased the rise time (fig. 2).

III. Plans

Future plans include testing the ten-bit A/D converter and looking further into the differences of the three filters. The difficulties will be to relate time domain responses of the filters to the frequency domain and to minimize the effects of the process on the measured data. Statistical analysis can also be applied to the measured data to minimize these process dependent effects however, more data will have to be obtained. I am also scheduled to take the Ph.D. Qualifying Examination this quarter.

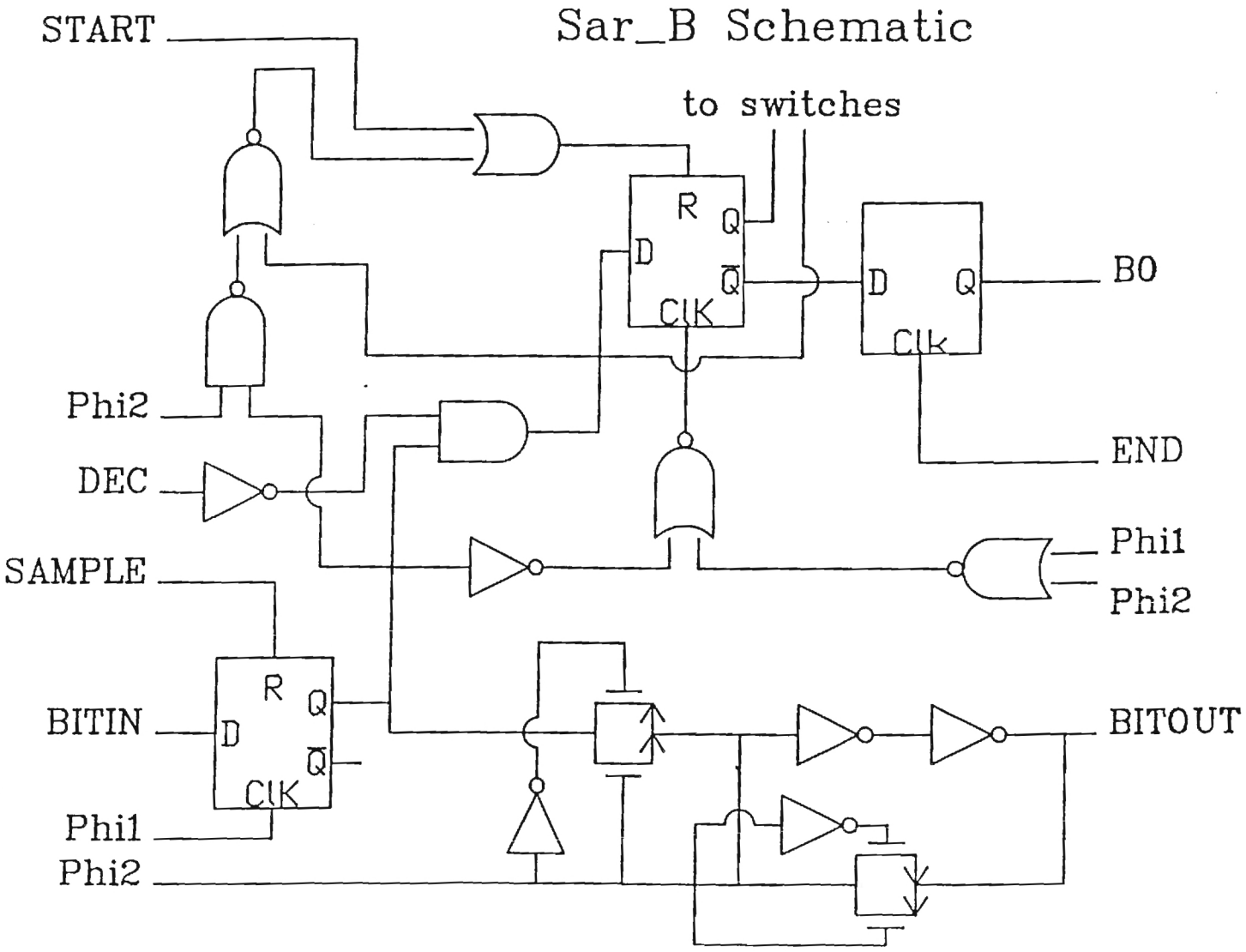

Sar_B Schematic
START
to switches
R
Q
D
Q̄
CLK
D
Q
CLK
B0
END
Phi2
DEC
SAMPLE
Phi1
Phi2
R
Q
BITIN
D
Q̄
CLK
BITOUT
Phi1
Phi2

FIGURE 1

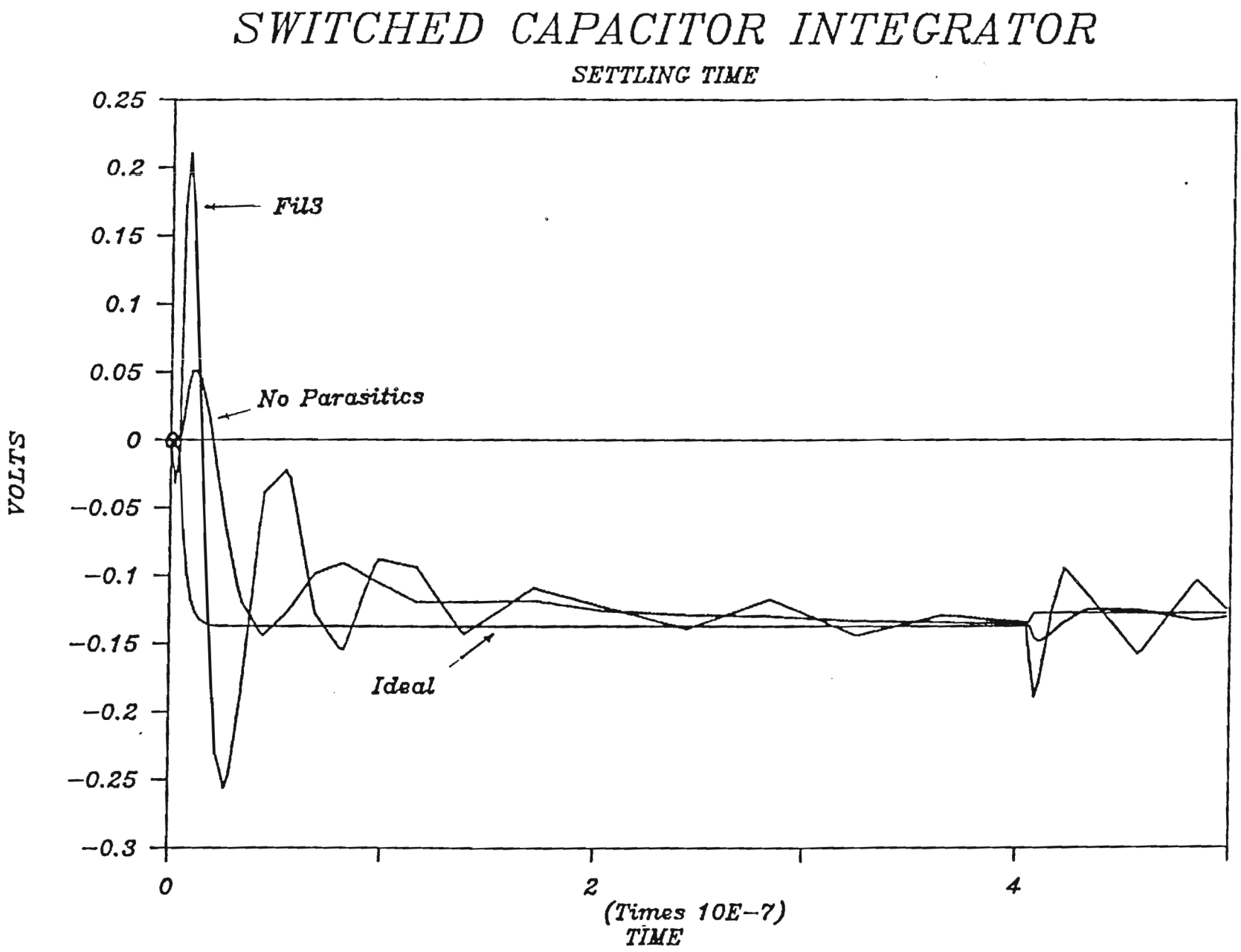

SWITCHED CAPACITOR INTEGRATOR
SETTLING TIME
0.25
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
VOLTS
Fil3
No Parasitics
Ideal
0
2
4
(Times 10E-7)
TIME

FIGURE 2

SRC Quarterly report on Spring 1988

Precision small signal model development for analog IC design

Kwang S. Yoon

July 5, 1988

1. Objectives:

To develop models and model methodology which result in the computer efficient, accurate analog small signal models for short-channel MOSFETs, including the submicron devices.

2. Accomplishments:

The benchmark of the table look-up model has been achieved, using the operational amplifier with the minimum feature size of 1.0um. The circuit diagram of the opamp with device aspect ratio is shown in Fig. 1. Table 1 illustrates that the accuracy of table look-up model is within 10% to predict the circuit performance such as open loop gain and output resistance of the operational amplifier, which is more accurate than BSIM model by an order of magnitude. Device size, M1(14.4um/1.6um) and M7(166.4um/1.6um) were used to extract the table look-up and BSIM model parameters for both n-channel and p-channel MOSFET, respectively.

In order to model and benchmark the intrinsic capacitances, it was necessary to layout the test structure of single n-channel/p-channel devices with the different W/L ratios, a super operational amplifier with the short-channel device, an unbuffered two stage opamp, several ring oscillators, as shown in Fig. 2. This layout has been submitted to MOSIS 1.6um CMOS n-well bulk process.

The developed table look-up model has been applied to simulate the performance of a short-channel cascode operational amplifier designed by one of SRC member companies. Several devices, including n-channel and p-channel devices (1.5um CMOS process), were extracted for table look-up model across the whole wafer. The simulated results of the open loop gain, output resistance, and power dissipation of the cascode opamp were consistent, although the table look-up model produced the inaccurate circuit performance which is attributed to the incorrect model parameter extraction.

3. Plans:

The instrinsic capacitances will be modeled and benchmark of capacitance modeling will be achieved in terms of the device and circuit level. The performance of the cascode opamp will be simulated after the table look-up model parameter extraction is modified correctly.

4. Publications/presentation:

"A Precision Model for Analog Circuits," NUPAD II Workshop, May 9-10, 1988, San Diego, CA.

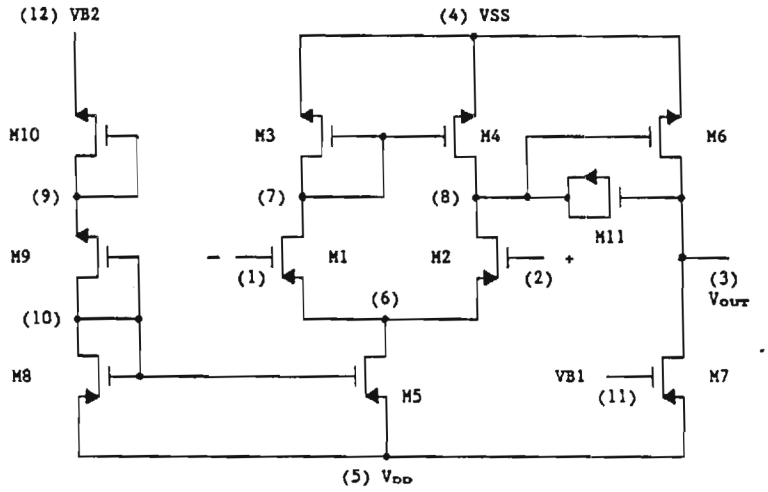
OPAMP	A_{VH}	A_{VT}	A_{VB}	T.L.U. ERROR(%)	BSIM ERROR(%)
#1	295.5	287.5	387.6	2.71	31.17
#2	280.5	275.4	378.6	1.82	29.63
#3	293.4	266.3	379.6	9.24	29.38
#4	293.4	311.4	381.6	6.13	30.06
#5	322.5	292.4	406.2	9.33	25.95
#6	288.4	274.8	349.9	4.72	21.32
AVERAGE	295.6	284.6	380.6	3.72	28.74

(a)

OPAMP	R_{OH}	R_{OT}	R_{OB}	T.L.U. ERROR(%)	BSIM ERROR(%)
#1	18.33K	18.69K	7.27K	1.96	60.34
#2	13.30K	14.03K	6.27K	5.49	52.86
#3	15.69K	16.92K	8.34K	7.84	46.85
#4	16.87K	16.66K	8.14K	1.24	51.75
#5	18.14K	20.15K	8.04K	11.08	55.68
#6	14.52K	15.07K	7.83K	3.79	46.07
AVERAGE	16.14K	16.92K	7.65K	4.83	52.60

(b)

Table 1. The comparisons of the simulated data from table look-up and BSIM models against the experimental data for the performance of (a) the open loop gain and (b) output resistance of the opamp



GEOMETRIC DIMENSION W/L (IN MICRONS)	
DEVICE	W/L
M1	14.4/1.6
M2	14.4/1.6
M3	1.6/1.6
M4	1.6/1.6
M5	4.8/1.6
M6	100.8/1.6
M7	166.4/1.6
M8	4.8/1.6
M9	1.6/6.4
M10	1.6/6.4
M11	100.8/100.8

Fig.1. Circuit diagram of the unbuffered two stage opamp with the device aspect ratio.

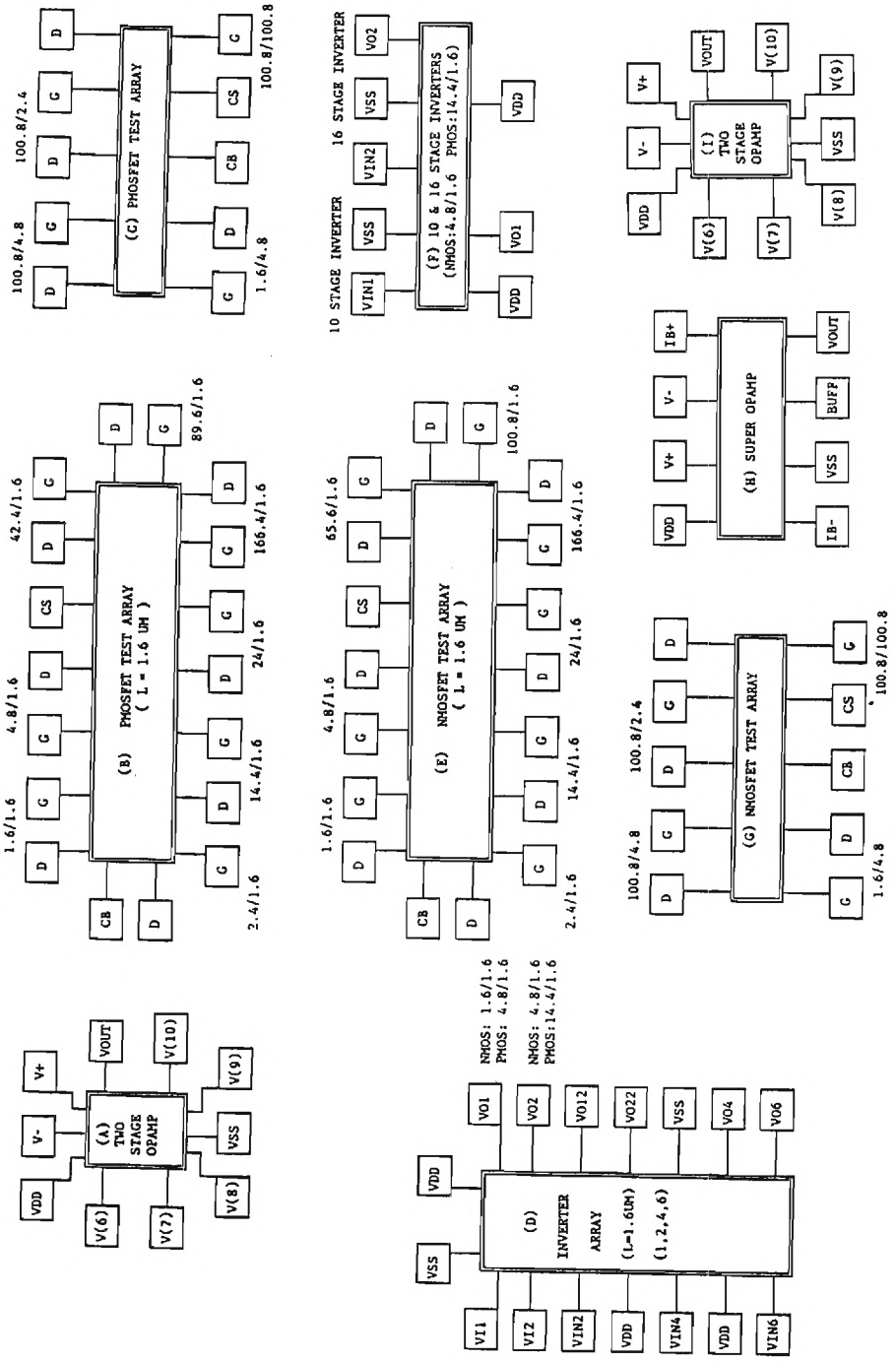


Fig. 2. The floor plan of the layout to benchmark the intrinsic capacitances of short-channel MOSFET devices.

8-BIT A/D CONVERTER SIMULATION

Anna Yan

July 4, 1988

Accomplishments

The goal of the spring quarter was to use IGSPICE and SABER to simulate the redesigned 4-bit A/D converter and to compare the results from both software programs.

In the process of the simulation with IGSPICE, it was found that extra level changes in the output of the Sar_B existed when the bit should be "0". With adding several gates to the Sar_B, the problem was successfully overcome. The final simulation results from IGSPICE were exactly as expected.

In order to simulate the converter using SABER program, several digital gate behavioral models were developed in MAST language, such as AND gate, NOR gate, inverter and D latches with/without reset signal. The switch behavioral model was created too. The function of this model is based on the assumption that the output is connected to the one of the two inputs to be transmitted, depending on the control signal. With these models and others from Saber template library, the circuit consisting of Sar_A and 4 Sar_Bs was simulated successfully.

The problems involved in using SABER were:
1. Because of errors in the SABER software, it seems impossible to simulate the whole circuit;
2. A lot of problems in simulation were due to the original D latch model was discontineous. So it is very important to create the continous behavioral models.

The comparisions between IGSPICE and SABER were made detailly by Harry Li in the design review report.

Plans

In the summer quarter, the A/D converter will be simulated by using the new version SABER software. The results will be compared again with those from IGSPICE.

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Phillip E. Allen	School of Electrical Engineering Georgia Tech, Atlanta, GA 30332

REPORT TITLE
Quarterly Report - June 1988 - August 1988

REPORT AUTHOR(S)
Phillip E. Allen

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None

B. Have the research results in the attached report been previously published or presented? [ ] Yes [X] No If yes, please check box(es) as appropriate:

Date (mo/day/yr)

[ ] SRC report: SRC Publication ID Number _____ _____

[ ] Thesis/Dissertation: Author _____ _____

[ ] Publication: Name of Journal _____ _____

[ ] Presentation: Location _____ _____

[ ] Software Manual: Title & Version _____ _____

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If yes, by whom?

Name(s) Phillip E. Allen

Title(s) Professor

Organization(s) Georgia Tech

Date Reviewed November 22, 1988

Patent Search Done? [ ] Yes (Date _____) [X] No [ ] In Progress

D. Current Status:

[ ] Invention Disclosure: Submitted to _____

[ ] Patent Application: US Serial No. & Filing date: _____

[ ] Issued Patent: Patent No. & Issue date _____

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Phillip E. Allen
Schlumberger Professor

Name and Address of Organization
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

REPORT TITLE

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REPORT AUTHOR(S)

Phillip E. Allen

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If an abstract of this paper has already been submitted to the SRC for approval, please check the box and give the SRC Publication ID number, if known. [ ] Abstract was previously submitted SRC Publication ID_____

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November 15, 1988

MEMORANDUM

TO: Jeff Hilbert, Program Manager, Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, June 1, 1988 to August 31, 1988, SRC Project No. 84-07-051; "Analog CAD Methodology"

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This research effort involves 6 PhD students. The students are Pjung Choi, Peter Flur, Seong Hong, Harry Li, Alan Mantooth, and Anna Yan. Juvena Loo and Kwang Yoon were both working in industry this quarter. A brief summary of the research results of the above students follows.

Generalized macromodeling approaches have been developed and applied to continuous and discrete filters. This modeling is used to implement frequency domain performance in the phase locked loop models. The major electrical parameters of the PLL including conversion gain of the phase detector, frequency sensitivity of the VCO, and loop filter transfer function can be implemented into the PLL macromodel. Efforts to develop a macromodel for a digital phase locked loop are in progress.

An ac sensitivity analysis capability has been implemented in SPICE-PAC and linked with the analog cell compiler. This analysis is used to provide information on reducing the influence of placement and routing parasitic influence on the performance of analog circuits. The influence of placement and

routing on the performance of analog blocks has been studied experimentally using the AIDE2 program to generate three electrically identical third-order filters with different placement and routing.

One of the new efforts which has been developed during the summer is behavioral modeling. The feedback from the SRC Design Review in June has been used to create a new behavioral modeling methodology based on nonlinear partial differential equations. This methodology has been implemented into SABER to obtain an accurate and CPU efficient static and dynamic model for a comparator.

The 4-bit successive approximation A-D converter simulated by IGSPICE was simulated on SABER to compare the two programs. The 8-bit version was also simulated on SABER but not on IGSPICE. SPICE-PAC was applied to the same problem resulting in much quicker simulation times. Unfortunately, the simulation level was not identical (logic level in SPICE-PAC and gate level in IGSPICE). Present efforts are directed to being able to make an equivalent comparison.

Report Organization

Each of the individuals working on this research program during the Summer 1988 quarter have written a brief summary of their efforts. These summaries follow this page. The research topic and student are listed as follows:

Macromodeling for Analog Circuits and Systems	Pyung Choi
Mixed Mode Simulation Using Spice-PAC	Peter Flur
Automated Layout of Analog Circuits	Seong Hong
Performance Oriented CAD Methods and Studies	Harry Li
Behavioral Modeling of Analog Circuits	Alan Mantooth
8-Bit A/D Converter Simulation	Anna Yan

Budget Expenditures

The personnel supported by SRC during this quarter include Dr. Allen, Pyung Choi, Seong Hong, and Alan Mantooth (SRC Fellow). Anna Yan who worked on SRC research was supported from the Schlumberger Chair funds. Peter Flur was supported from returned overhead. The SRC expenditures for this period are listed below:

Expenditure Category	June 1988	July 1988	August 1988	Totals
Personal Services	$2,880.00	$7,590.00	$11,450.00	$21,920.00
Fringe Benefits	$0.00	$1,476.00	$2,460.00	$3,936.00
Materials & Supplies	$595.00	$289.00	$699.00	$1,584.00
Travel	$0.00	$0.00	$1,121.00	$1,121.00
Computer	-	-	-	-
Overhead	$2,085.00	$5,613.00	$9,438.00	$17,137.00
TOTALS	$5,562.00	$14,968.00	$25,168.00	$45,698.00

MACROMODELING FOR COMPLEX NONLINEAR ANALOG CIRCUITS AND SYSTEMS

Pyung Choi
Quarterly Report for Summer 1988

Objectives

1. **Macromodel for Phase Locked Loop** - Develop macromodel for Analog Phase Locked Loop (APLL) and Digital Phase Locked Loop (DPLL) which will predict dynamic loop behavior such as pull-in time, capture and lock range, and loop stability.

2. **Macromodeling Technology** - Develop modeling techniques for automatic generation of "Drop-In" macromodels for functional parts of complex nonlinear analog circuits and systems.

Accomplishments

Research activities during the summer quarter have been emphasized to the development and programming of a generalized macromodel approaches for Continuous Filtering Functions (CFFs) and Discrete Filtering Functions (DFFs). As a result it, a generalized macromodeling technique for CFFs and DFFs has been developed and programmed for automatic generation of functional level models which are valid to SPICE.

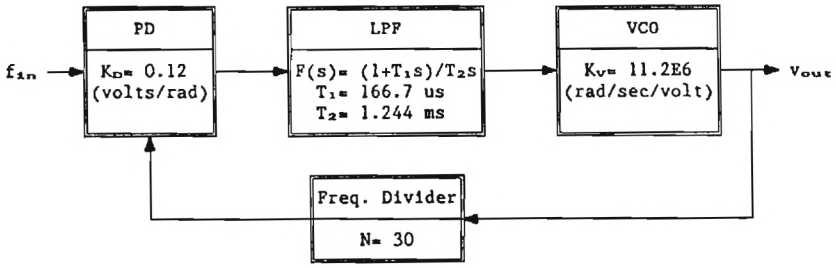
The s-domain PLL macromodel which is derived from the CFF modeling technique allows the designer to predict or to simulate PLL stabilities such as gain and phase margins. The major electrical parameters of the PLL including conversion gain of phase detector, frequency sensitivity of VCO, and loop filter transfer function can be implemented into the macromodel. Besides of this application, the generalized CFF macromodel approach is useful to model the linear parts of complex nonlinear analog circuits and systems.

The DFF macromodeling technique has the same basic algorithm as that of continuous functions. The difference between s and z-domain macromodels is that Type I Direct transform Discrete Integrator (Type I DDI) is used as the unit integrator instead of 1/s integrator in the s-domain. These z-domain macromodels allows SPICE to simulate switched capacitor networks without any internal modifications. Also SC networks which transfer functions are known can be analyzed without any circuit implementations.

The EXclusive-OR (EX-OR) type phase detector macromodel has been developed. The macromodel consists of a summer and a PWL function sub-model. The performances of the model are well matched to theoretical values.

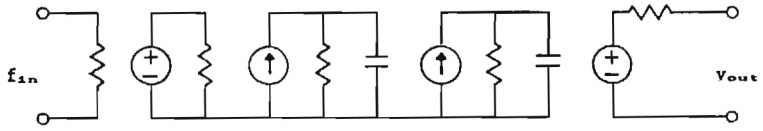
Plans

The plans for the next quarter are: (1) Full development the APLL macromodel, (2) Development of frequency divider model, and (3) Proposal for Ph.D. dissertation.

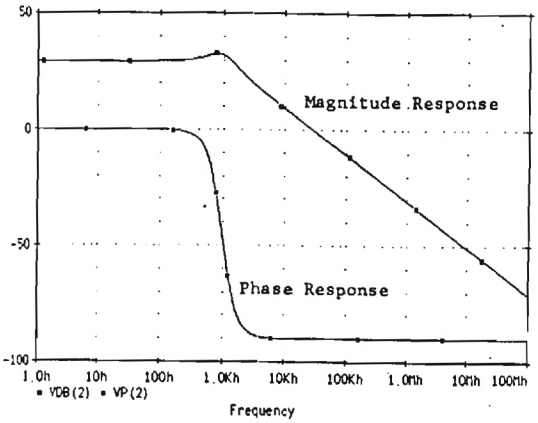


Damping Factor= 0.5 Loop Natural Frequency= 6000 (rads/sec)

(a) Functional Block Diagram of Example DPLL



(b) Macromodel for Example DPLL (Frequency-Domain)



(c) PSpice Simulation Results

Figure 1. Digital Phase-Locked Loop AC Macromodel

Normalized Butterworth
2nd order LPF

$$H(s) = \frac{1}{s^2+1.414s+1}$$

Forward Transform
Sampling Frequency
= 100 Hz

Normalized Butterworth
2nd order SC LPF

$$H(z) = \frac{1}{10000z^2-19858.6z+9859.599}$$

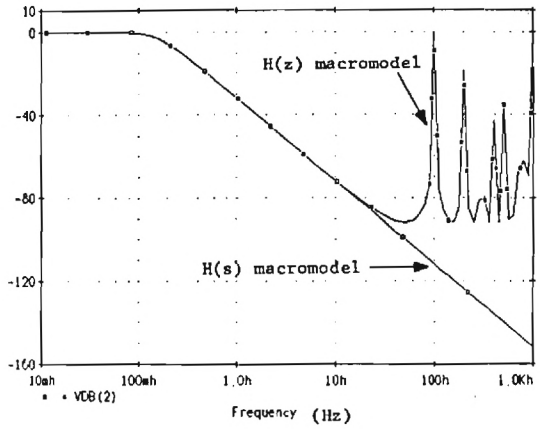


Figure 2. z-Domain Macromodel

Mixed Mode Simulation Using Spice-PAC
Peter W. Flur
September 7, 1988

Accomplishments

The goal of this research was to integrate a digital simulator with the Spice-PAC (SPPAC) simulator. SPPAC has an interface which allows a digital simulator to execute during the process of a Spice simulation. The analog-digital interface is accomplished by means of a "thresholder", which determines digital values to be passed to the digital simulator. The digital-analog interface works by means of "smoothers", which smooth out the hi-low and low-hi transitions of the digital simulator to allow the values to be used during analog simulation (see figure 1). The timing of the digital simulation is completely under the control of the analog simulation loop.

The transfer of data is accomplished using two sets of arrays passing inputs to the digital simulator, and passing outputs back to the analog simulator.

Before this work began, the only means of mixed-mode simulation in SPPAC was a hard-coded FORTRAN subroutine which emulated the digital circuitry.

The first task was choosing a digital simulator which could be modified to fit into the SPPAC environment. Due to time limitations, RSIM from Chris Terman at MIT was chosen. The code was integrated into the SPPAC environment so that a mixed mode simulation could be run. Once the integration was complete, the next task was to find a viable example to test the interface. A section of a pipelined A/D converter was chosen, and the encoder modeled in RSIM. The analog comparators were modeled using an ideal comparator. To date, the individual parts (analog and digital) have been simulated correctly, and the mixed-mode simulation has yet to be completed.

Plans

During the next quarter, I plan to complete the simulation of the A/D converter section to prove (or disprove) functionality. If the one section simulates properly, simulation times and results must be compared with IGSPICE and Saber. In addition, an hierarchical pipelined A/D converter must be simulated to evaluate execution times on a large mixed mode circuit. I also hope to extend the input language of RSIM to easily handle the mixed analog and digital circuits.

A simulator other than RSIM must be found to prove that the interfaces are not restricted to the RSIM environment. Preferably, a gate level simulator will be found.

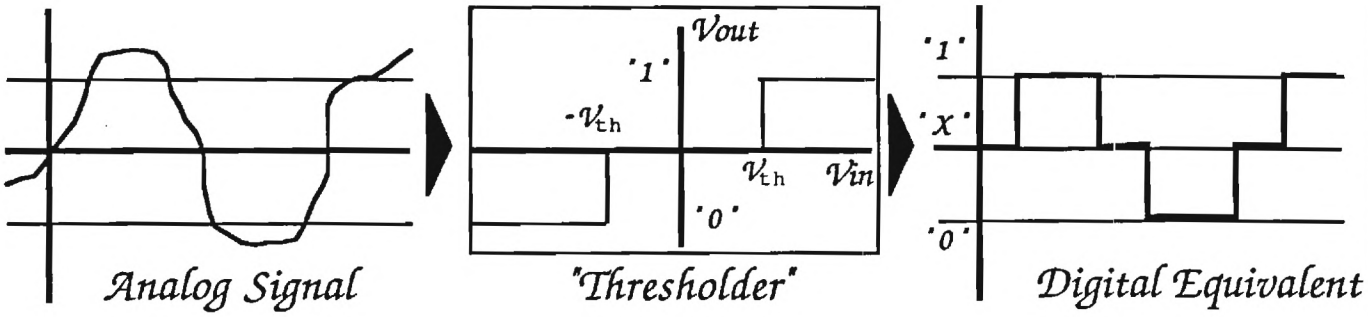
Potential Problems

The two largest forseeable problems are the lack of simulators available on the public domain that satisfy our requirements and interfacing and debugging with Dr. Zuberek at the Memorial University at St. Johns, Newfoundland.

Analog/Digital Interface in Spice PAC

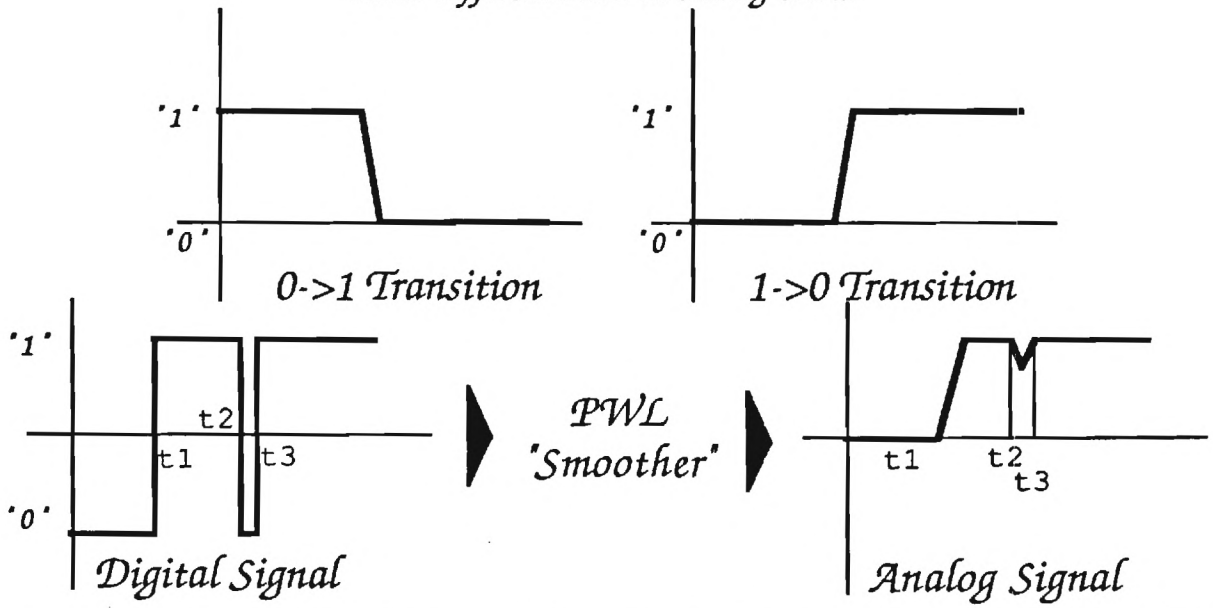
Analog to Digital Conversion

Analog to Digital is accomplished using 'thresholders' which convert levels in the analog world to digital values.



Digital to Analog Conversion

Digital to Analog conversion is done using 'smoothers' which smooth the digital 1->0 and 0->1 transitions using piecewise linear curves to allow differentiation in analog world



AUTOMATED LAYOUT OF ANALOG CIRCUIT

Seong K. Hong
Quarterly Report on Summer 1988

Objectives

To develop a software program which can take a SPICE input file and automatically create a layout which has been optimized according to a user specified performance by using the sensitivity analysis.

Accomplishments

The summer activity has been developing the sensitivity analysis program and simulation file generator based on the user specified performance, which can drive the automated component design methodology. The evaluation of normalized DC and AC (small signal) sensitivities with respect to layout parasitic resistances and capacitances has been implemented in the SPICE-PAC package and internally linked with the cell compiler. Figure 1 shows the interface of SPICE-PAC with cell compiler. With the information on the circuit structure from the user, the cell compiler generates the sppac_file depending on the user specified performance interactively. This file also includes the effects due to the layout parasitics on the interconnections between the devices. Up to this point, the user can specify several performances of op amp such as offset voltage, common mode range, gain bandwidth, and power supply rejection ratio. After running the SPICE-PAC with the file from cell compiler, the user can get the sensitivity analysis results which can be implemented to the placement and routing strategy. Figure 2 shows the examples of sensitivity analysis with respect to the layout parasitics depending on the different op amp performances: (a) offset for dc and (b) gain bandwidth for ac.

The implementation of the net tracing algorithm for the placement has been under development. So far, the program sorts the all devices by p and n type and traces the diffusion line from the power line. It should be improved in several aspects in the next quarter (See plans).

Plans

1. Optimization and estimation of bounding box depending on the aspect ratio given by user.
2. Implementation of the recognition rules of various configuration such as diff_amp and cascode type.

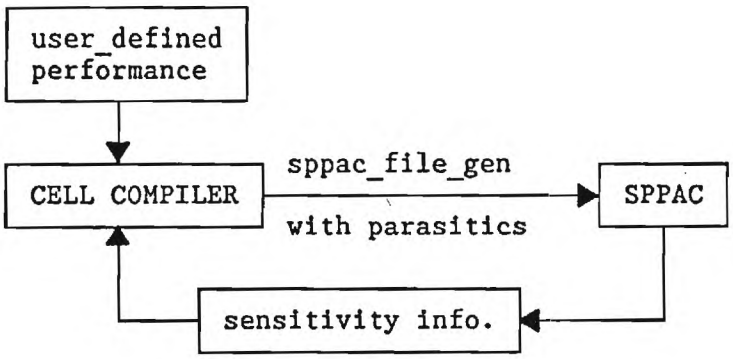


Figure 1. Interface of SPICE-PAC with cell compiler

***** DC SENSITIVITIES

	ELEM	V(7)
S/RM1d	1.00d+02	-1.41d-03
S/RM1g	1.00d+02	0. d+00
S/RM1s	1.00d+02	-1.10d-01
S/RM2d	1.00d+02	1.41d-03
S/RM2g	1.00d+02	0. d+00
S/RM2s	1.00d+02	1.10d-01
S/RM3d	1.00d+02	3.59d-02
S/RM3g	1.00d+02	3.59d-02
S/RM3s	1.00d+02	2.21d-01
S/RM4d	1.00d+02	-1.02d-03
S/RM4g	1.00d+02	1.38d-15
S/RM4s	1.00d+02	-2.26d-01
S/RM5d	1.00d+02	3.85d-05
S/RM5g	1.00d+02	0. d+00
S/RM5s	1.00d+02	4.06d-03
S/RM6d	1.00d+02	2.71d-05
S/RM6g	1.00d+02	2.30d-17
S/RM6s	1.00d+02	9.49d-03
S/RM7d	1.00d+02	-3.20d-03
S/RM7g	1.00d+02	0. d+00
S/RM7s	1.00d+02	-6.46d-03
S/RM8d	1.00d+02	3.50d-05
S/RM8g	1.00d+02	3.50d-05
S/RM8s	1.00d+02	2.10d-04
S/RM9d	1.00d+02	-3.03d-04
S/RM9g	1.00d+02	-3.03d-04
S/RM9s	1.00d+02	-1.58d-03
S/RM10d	1.00d+02	2.63d-18
S/RM10g	1.00d+02	0. d+00
S/RM10s	1.00d+02	0. d+00

(a) dc for offset

***** AC SENSITIVITIES

FREQ	S(RM1d).M	S(RM1g).M	S(RM1s).M	S(RM2d).M	S(RM2g).M	S(RM2s).M
1.00d+00	3.22d-05	1.00d-20	2.50d-03	3.30d-05	3.29d-10	2.57d-03
1.00d+01	3.22d-05	3.65d-10	2.50d-03	3.30d-05	3.29d-09	2.57d-03
1.00d+02	3.22d-05	3.65d-09	2.50d-03	3.31d-05	3.29d-08	2.57d-03
1.00d+03	3.24d-05	3.67d-08	2.51d-03	3.32d-05	3.29d-07	2.58d-03
1.00d+04	3.28d-05	3.72d-07	2.55d-03	3.37d-05	3.27d-06	2.63d-03
1.00d+05	3.25d-05	3.68d-06	2.52d-03	4.01d-05	3.23d-05	3.14d-03
1.00d+06	2.43d-05	2.75d-05	1.88d-03	1.16d-04	2.31d-04	9.18d-03

FREQ	S(RM3d).M	S(RM3g).M	S(RM3s).M	S(RM4d).M	S(RM4g).M	S(RM4s).M
1.00d+00	8.20d-04	8.20d-04	5.04d-03	2.38d-05	1.00d-20	5.27d-03
1.00d+01	8.20d-04	8.20d-04	5.04d-03	2.37d-05	1.42d-09	5.27d-03
1.00d+02	8.20d-04	8.20d-04	5.04d-03	2.38d-05	1.42d-08	5.27d-03
1.00d+03	8.24d-04	8.24d-04	5.06d-03	2.36d-05	1.42d-07	5.22d-03
1.00d+04	8.35d-04	8.35d-04	5.13d-03	2.28d-05	1.41d-06	5.04d-03
1.00d+05	8.28d-04	8.28d-04	5.08d-03	2.26d-05	1.39d-05	5.01d-03
1.00d+06	6.05d-04	6.05d-04	3.72d-03	1.92d-05	7.00d-05	4.34d-03

FREQ	S(RM5d).M	S(RM5g).M	S(RM5s).M	S(RM6d).M	S(RM6g).M	S(RM6s).M
1.00d+00	1.23d-08	1.00d-20	1.30d-06	2.27d-04	4.40d-10	7.96d-02
1.00d+01	1.23d-08	1.00d-20	1.30d-06	2.27d-04	4.41d-09	7.96d-02
1.00d+02	1.23d-08	2.22d-12	1.30d-06	2.28d-04	4.41d-08	7.96d-02
1.00d+03	1.27d-08	2.31d-11	1.34d-06	2.28d-04	4.41d-07	7.96d-02
1.00d+04	2.91d-08	2.70d-10	3.07d-06	2.28d-04	4.41d-06	7.96d-02
1.00d+05	2.60d-07	1.51d-08	2.74d-05	2.93d-04	4.35d-05	7.86d-02
1.00d+06	1.96d-06	1.12d-06	2.05d-04	9.66d-04	2.22d-04	4.88d-02

FREQ	S(RM7d).M	S(RM7g).M	S(RM7s).M	S(RM8d).M	S(RM8g).M	S(RM8s).M
1.00d+00	2.69d-02	1.84d-10	5.42d-02	2.77d-13	2.77d-13	1.66d-12
1.00d+01	2.69d-02	1.84d-09	5.42d-02	2.77d-12	2.77d-12	1.66d-11
1.00d+02	2.69d-02	1.84d-08	5.42d-02	2.77d-11	2.77d-11	1.66d-10
1.00d+03	2.69d-02	1.84d-07	5.42d-02	2.75d-10	2.75d-10	1.65d-09
1.00d+04	2.69d-02	1.84d-06	5.42d-02	2.67d-09	2.67d-09	1.61d-08
1.00d+05	2.68d-02	1.83d-05	5.42d-02	2.63d-08	2.63d-08	1.58d-07
1.00d+06	2.62d-02	1.80d-04	5.30d-02	1.41d-07	1.41d-07	8.49d-07

FREQ	S(RM9d).M	S(RM9g).M	S(RM9s).MS	(RM10d).MS	(RM10g).MS	(RM10s).M
1.00d+00	2.08d-11	2.08d-11	1.09d-10	8.86d-20	1.00d-20	1.30d-14
1.00d+01	2.08d-10	2.08d-10	1.09d-09	8.86d-18	4.65d-16	1.31d-12
1.00d+02	2.08d-09	2.08d-09	1.09d-08	8.82d-16	8.06d-14	1.32d-10
1.00d+03	2.06d-08	2.06d-08	1.08d-07	6.46d-14	5.23d-11	1.04d-08
1.00d+04	2.01d-07	2.01d-07	1.05d-06	3.05d-13	2.36d-09	4.63d-08
1.00d+05	1.98d-06	1.98d-06	1.03d-05	2.63d-12	2.92d-08	6.41d-08
1.00d+06	1.06d-05	1.06d-05	5.55d-05	2.80d-11	8.53d-07	9.00d-07

(b) ac for gain bandwidth

Figure 2. Sensitivity analysis depending on different performances

SRC Quarterly Report
Harry W. Li
Summer 88

I. Accomplishments

Due to a shortened summer quarter, the entire quarter was needed in order to take the Ph.D. Qualifying Examination. A paper entitled "A Survey of Automatic Layout Tools Suitable for Analog Circuits and Systems" was written as part of the exam.

II. Plans

The goal of the fall quarter will be to determine if there is a need for automated analog systems layout. This will include examining the effects of parasitics and crosstalk between interconnections of an analog block and to what extent the performance of the block is influenced by these effects. Also, a model which includes parasitics due to interconnect will be investigated.

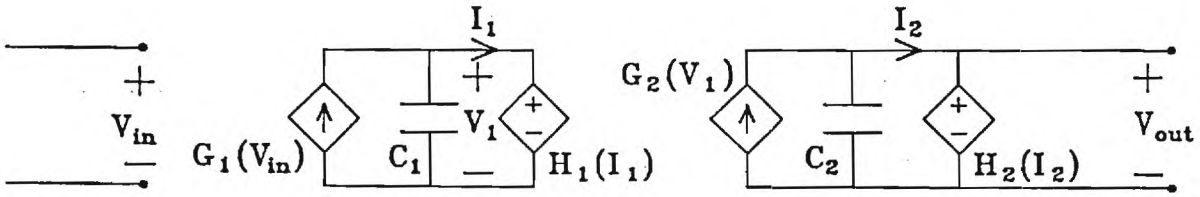
Analog Behavioral Modeling

H. Alan Mantooth

September 12, 1988

Accomplishments

The primary emphasis of this research during the previous quarter (Spring 1988) was involved with automatic behavioral model generation. However, after further discussions with SRC and some of its member companies, this research has taken a slightly new direction. The current focus of this research is on generalized behavioral modeling techniques for analog circuits and systems. During the summer quarter, work was initiated on the behavioral model of a voltage comparator using more general techniques than reported previously at the Georgia Tech SRC Design Review in June. The following circuit is a macromodel of the two-stage comparator from which nonlinear differential equations (NDE's) are derived. These NDE's (Eqs. 1 and 2) are implemented in the MAST modeling language for use with the Saber simulator.



$$I_1 + C_1 * d(V_1)/dt = G_1(V_{in}) \quad (1)$$

$$I_2 + C_2 * d(V_{out})/dt = G_2(V_1) \quad (2)$$

where $G_1(V_{in})$, $H_1(I_1)$, $G_2(V_1)$, and $H_2(I_2)$ are nonlinear functions. The nonlinear functions above are extracted from SPICE simulations of the actual two-stage comparator given on the next page. The two voltage-controlled current sources represent the short circuit current of each respective stage. The current-controlled voltage sources represent the open circuit voltages of each respective stage. The capacitances determine the two dominant poles of the comparator. Comparisons of the ac, dc, and transient responses between the behavioral model simulated on Saber and the SPICE simulation of the comparator are also shown on the next page. The CPU times for each are given below these curves.

Plans

The modeling techniques presented above will continue to be pursued. The next step is to attempt to incorporate more nonidealities into the comparator behavioral model and to resolve any discrepancies evident in the curves shown above. Then, the modeling techniques will be generalized, if possible.

Publications

The research on automatic behavioral model generation was presented at the Georgia Tech SRC Design Review held at Georgia Tech on June 17, 1988. It met with a favorable response from those attendees from industry and SRC.

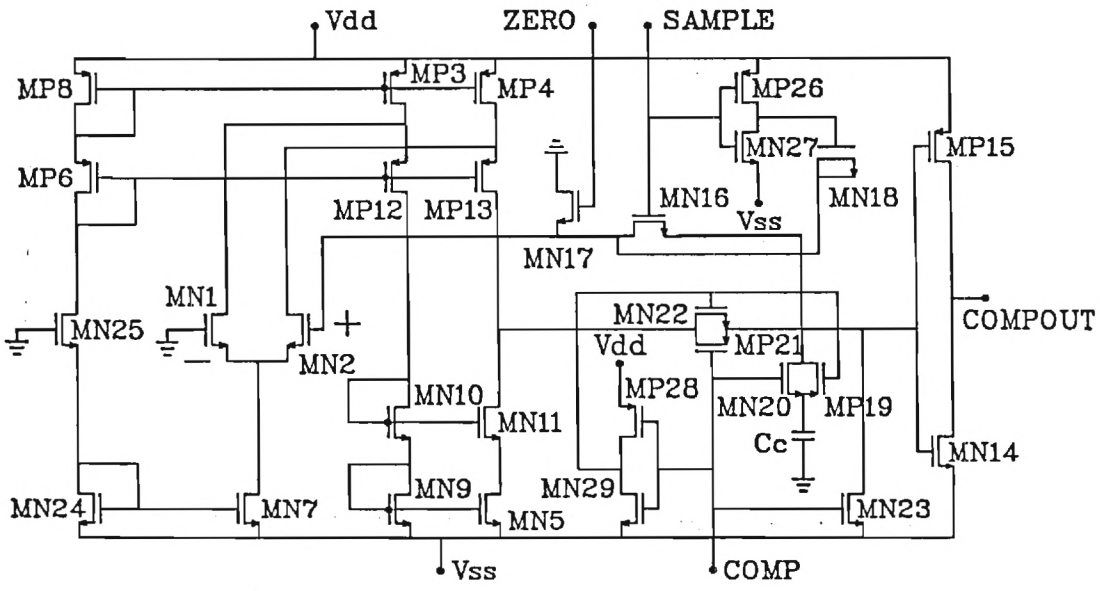


Fig. 1 AIDE2 Comparator/Op Amp.

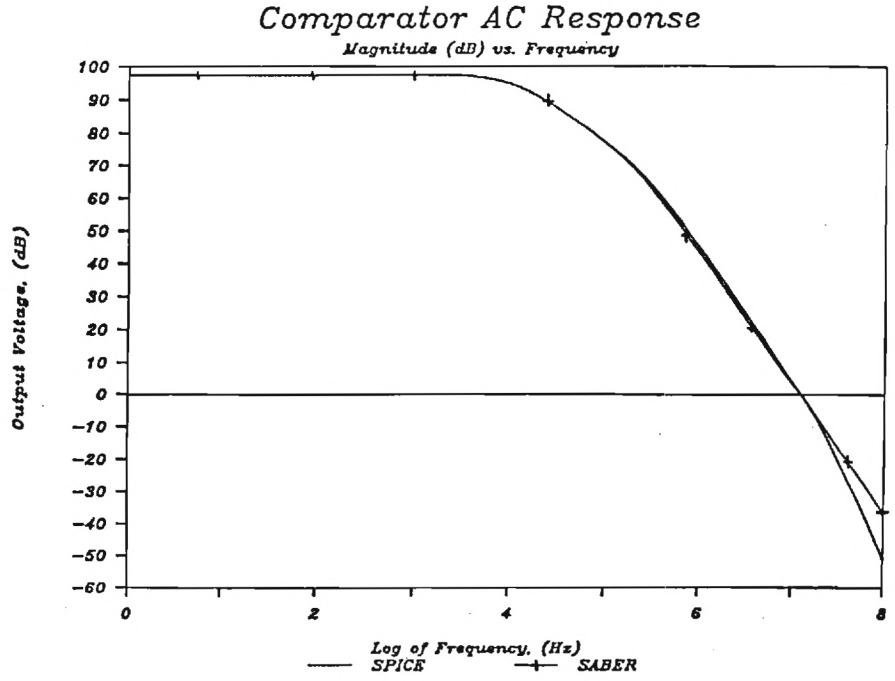


Fig. 2 Comparator ac responses (SPICE vs. Saber).

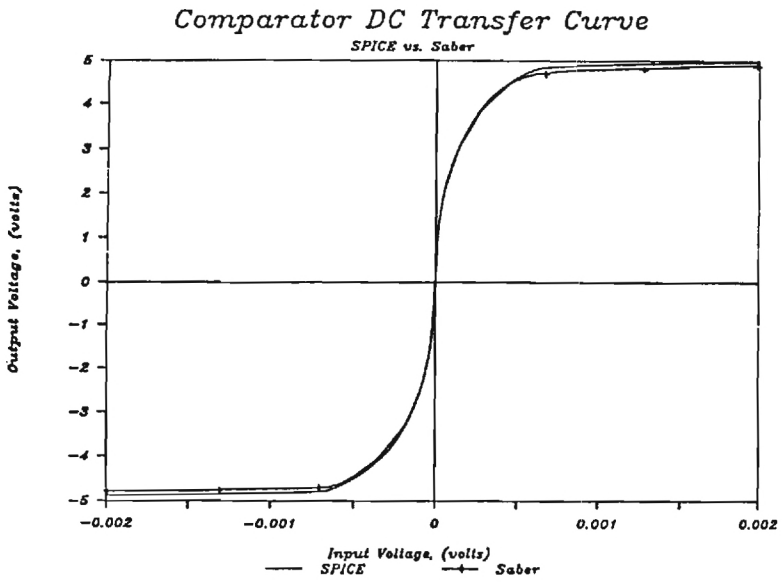


Fig. 3 Comparator dc transfer curves (SPICE vs. Saber).

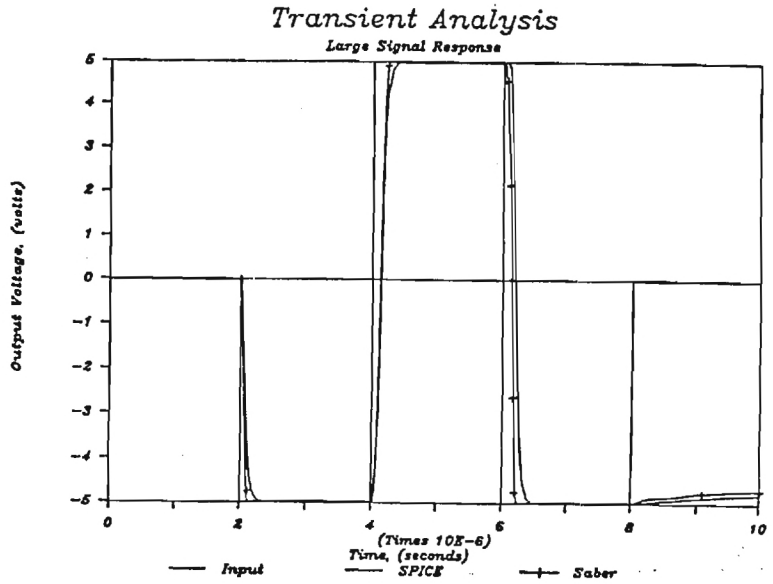


Fig. 4 Comparator transient responses (SPICE vs. Saber).

Analysis	Saber (uVAX seconds)	SPICE (uVAX seconds)
.OP	1.00	16.53
.DC	17.60	150.60
.AC	9.63	40.40
.TRAN	29.40	534.30
Totals	57.63	741.83

8-BIT A/D CONVERTER SIMULATION

Anna Yan
September 10, 1988

Objectives

1. Simulate 4-bit A/D converter by SABER.
2. Understand how the SPICE-PAC (SPPAC) works and use its function of "external", "run-time" control of the transient analysis to simulate the mixed-mode circuits.

Accomplishments

The 4-bit A/D converter simulated in previous quarter was simulated again with the new version 2.1 of SABER software. The simulation time for the digital part had great difference by using two different kinds of switch model in sar_b blocks. It took about 3 hours to run 35 us transient analysis with MOSFETs but only 27 minutes with behavioral switch model which was developed during Spring Quarter. The entire circuit of 4-bit A/D converter was also tried but the result of transient analysis was incorrect because the comparator model worked improperly.

To complete the second task, the analog parts of a 4-bit and a 8-bit converter were examined by SPPAC. The "external" subroutines for digital parts were written by Dr. Zuberek in FORTRAN code. During process of simulating the whole circuits (4-bit and 8-bit converters), those subroutines were called by SPPAC to determine digital values. By this method both 4-bit and 8-bit A/D converters were successfully simulated and the simulation time was found much less than that by IGSPICE. The comparisons are made in following table:

converter	simulation time	
	SPPAC	IGSPICE
4-bit	21 min.	6 hours
8-bit	35 min.	??

Since the interfaces between analog and digital parts have been updated by Dr. Zuberek at the end of the quarter, the subroutine for digital part of the converter needs to be changed too. Now the work of rewriting program has been done but in the simulation of the entire converter circuit some new problems have been met. These problems need to be solved in the next quarter.

Plans

1. Complete 4-bit and 8-bit A/D converters with SPPAC.
2. Continue simulating A/D converters using SABER.

E-21-636

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REPORT AUTHOR(S)

Phillip E. Allen

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ABSTRACT OF CONTENTS OF THIS SUBMISSION (must be in the space below or on a separate sheet of paper attached to this form) This report describes the research performed for the Semiconductor Research Corporation at Georgia Tech during the period from September 1, 1987 to August 31, 1988. The major accomplishments of this research are the development of precision analog models for short channel MOSFETs, higher level models for analog circuits, and a compiler for automated layout of analog circuits. In addition, mixed analog-digital simulation was performed on a 4-bit and 8-bit successive approximation, A/D converter using existing software programs. A new research activity involves the evaluation of using the SPICE-PAC simulation program as a mixed analog-digital simulator.

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ANNUAL PROJECT REPORT

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February 28, 1989

ANALOG CAD METHODOLOGY

Prepared for

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ANALOG CAD METHODOLOGY

Abstract

This report describes the research performed for the Semiconductor Research Corporation at Georgia Tech during the period from Sept. 1, 1987 to August 31, 1988. The major accomplishments of this research are the development of precision analog models for short channel MOSFETs, higher level models for analog circuits, and a compiler for automated layout of analog circuits. In addition, mixed analog-digital simulation was performed on a 4-bit and 8-bit successive approximation, A/D converter using existing software programs. A new research activity involves the evaluation of using the SPICE-PAC simulation program as a mixed analog-digital simulator.

The precision analog modeling uses a table look-up approach which permits adjustable dc and ac accuracy and has the same CPU times as BSIM or the level 2 model of SPICE. The higher level modeling is divided into macromodels and behavioral models. Macromodels have been developed and applied to model an analog phase-locked loop. Behavioral models are based on nonlinear differential equations and have been used to model a comparator with accuracy approaching the device level simulation and a speed-up factor of 10. Mixed analog-digital simulation was performed on a successive approximation A/D converter generated by an A/D compiler program. The compiler for analog circuit layout uses sensitivity of the circuit performance with respect to the parasitics to place and route components to best achieve a desired performance goal.

Plans include the completion of the above projects and the development of a focus on analog modeling and simulation. Model complexity, adaptability, and hierarchical relationships are important issues. These will be important areas in addressing the problem of analog IC and analog testability.

TABLE OF CONTENTS

1.0 INTRODUCTION

This research was designed to support and help achieve the general SRC goals in the design sciences area particularly in analog circuits and systems design. The objective of this research in the area of computer aided design and modeling of analog integrated circuits is to develop methodologies for analog circuit design which can be implemented by the computer. This research is designed to be used with digital CAD tools to design, simulate, and layout signal processing containing both analog and digital circuits.

While the organization used in this report is based on the proposal [1], the results are better understood from the viewpoint illustrated in Fig. 1. In this figure, the activities have been separated into design, modeling, simulation, and layout. Each category can be further divided hierarchically into devices, circuits, and systems. In this report, the higher level modeling

	Design	Modeling	Simulation	Layout
Device	-	Precision Analog Models	Multilevel	
Circuits	Automated Circuit Design	Macromodeling using SPICE	Mixed Analog and	Automated Cell Compiler
Systems	ADDAC	Behavior Models using SABER	Digital	

Fig. 1 - Classification of the research in Analog CAD Methodology.

activities are included within the simulation research description.

This report describes the research performed for the Semiconductor Research Corporation at Georgia Tech during the period from September 1, 1987 to August 31, 1988. The major accomplishments of this research are primarily in the area of modeling. They include the use of a table look up model to model complex

analog circuits with an order of magnitude more precision and less CPU time then existing analog device level models. Macromodels using SPICE primitives have successfully been implemented to simulate analog phase locked loops including nonlinear and linear behavior. A third modeling effort has resulted in behavioral models of analog circuits implemented on SABER which maintain desired accuracy with a reduction in CPU time of an order of magnitude compared with device level simulation.

2.0 PERFORMANCE ORIENTED CAD TECHNIQUES

Performance oriented CAD techniques involve the development of CAD techniques which attempt to provide automated or partially automated methods of designing analog circuits with maximum performance and minimum area requirements. In this research, this objective was approached by examining the limitations of two CAD programs - AIDE2 [2] and ADDAC [3]. In addition, a physical cell compiler is being developed to provide a method of converting a SPICE input circuit description into a physical layout which has been optimized in the performance designated by the user. The research results under the category of performance oriented CAD techniques will be presented in the subcategories of improved discrete-time modeling and comparison of a fifth-order benchmark filter designed by AIDE2, a comparison of electrical identical by physically different circuits designed by AIDE2, the measurement and simulation of a 8-bit successive approximation analog-digital converter designed by ADDAC, and the present status of the automated analog cell compiler.

2.1 Improved Modeling for Discrete Time Simulation

The objective of this research is to enhance the performance of the AIDE2 CAD platform by improving its simulation capability for switched capacitor circuits. AIDE2 presently provides a SPICE simulation input file for each

switched capacitor circuits that is designed. This simulation is used to insure that the circuit will meet the desired performance. Transmission lines are used to model the switched capacitors which employ a two-phase, nonoverlapping clock. However, the op amp models are ideal in that they only incorporate finite gain. This research added the capability to model the op amp gain-bandwidth, the op amp power supply injection, and the op amp noise. These model features were employed in the discrete-time frequency domain to be able to better predict the performance of switched capacitor filters.

The gain-bandwidth of the op amp was modeled by the use of a first order switched capacitor filter to implement the pole. Fig. 2 shows the implementation of the pole. The pole frequency is designed by the relationship

$$\text{Op Amp Pole} = (f_C C_2)/C_3 \tag{1}$$

where f_C is the clock frequency. Fig. 2 is actually converted in SPICE to a model containing controlled sources, capacitors, and transmission lines. Fig. 3 shows the frequency response of the experimental and simulated op amp using the macromodel of Fig. 2.

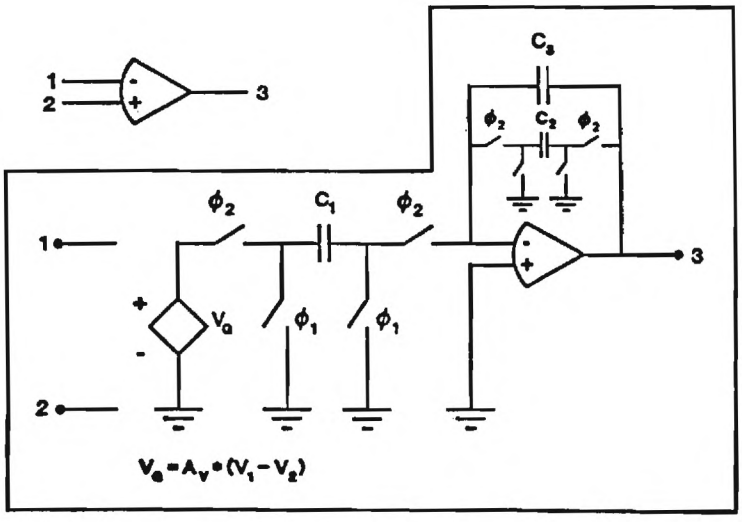


Fig. 2 - Switched capacitor implementation of finite op amp pole.

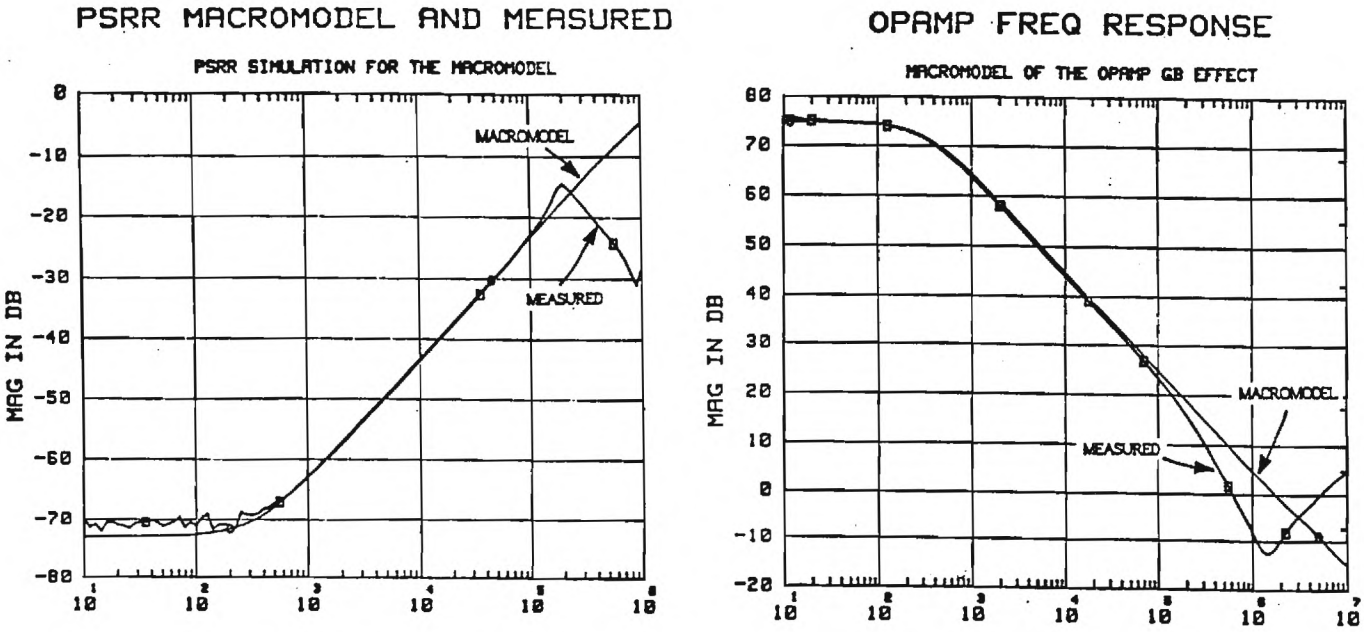


Fig. 3 - Frequency response of the op amp including both differential gain and power supply rejection ratio.

The controlled source in Fig. 2 designated at $A_{dd}*V_4$ is used to model the power supply injection where node 4 is assumed to be the power supply of concern. The results of the model and the measured power supply rejection ratio are shown in Fig. 3 along with the differential frequency response.

The noise of the op amp can be modeled as thermal noise and flicker noise. To generate the flicker noise a semiconductor diode is biased with a dc current source as shown in Fig. 4. The diode flicker noise voltage is used to control a voltage source in series with the noninverting op amp input. The thermal noise is modeled by the resistor R_n whose value is selected to match the experimental

thermal noise. Since R_n is not in the switched capacitor signal path, Fig. 4 is compatible with the discrete time SPICE simulation of switched capacitor circuits. Fig. 5 gives the experimental and simulation noise measurement of the op amp using the model of Fig. 4.

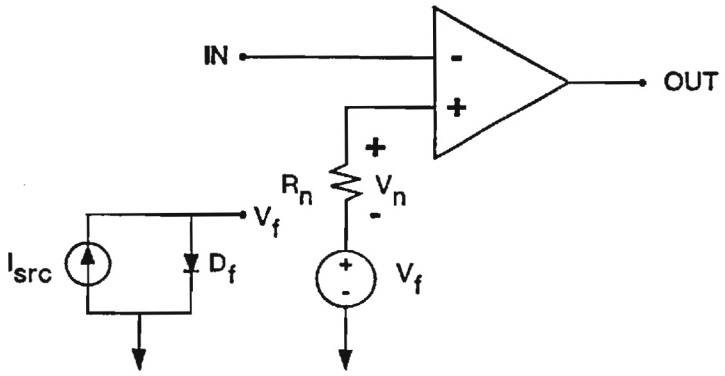


Fig. 4 - Op amp noise model for thermal and flicker noise.

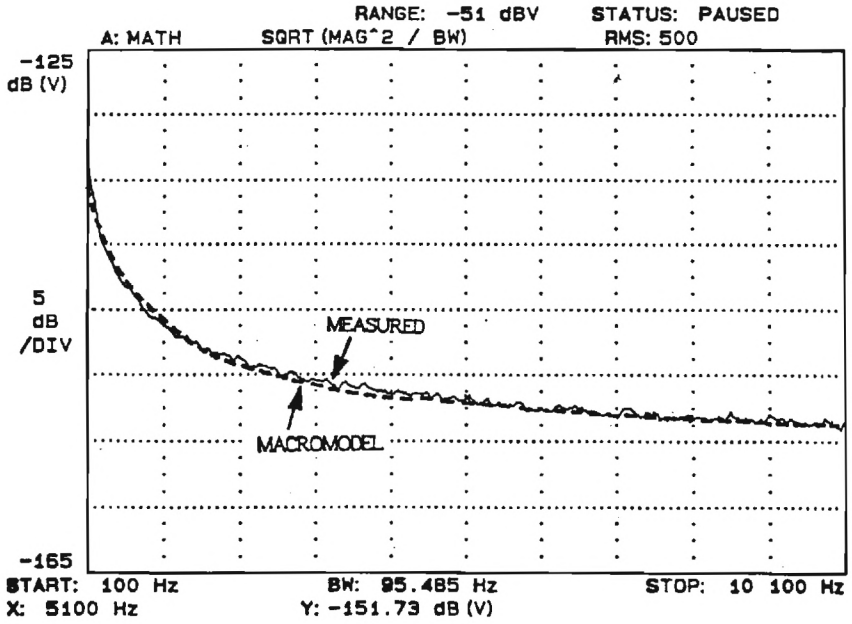


Fig. 5 - Experimental and simulated noise performance of the op amp.

The above model was used in the AIDE2-generated SPICE analysis of a fifth order PCM receive filter that was designed and fabricated using the AIDE2 program. This filter is equivalent to the Harris HC5512C integrated circuit and was fabricated using the same Harris process. The experimental results of the HC5512A and the AIDE2 designed circuit are compared with the simulation predicted performance in Figs. 6, 7, and 8. Fig. 6 compares the frequency response of the filter. Fig. 7 compares the power supply rejection ratio and Fig. 8 compares the noise.

The frequency response agrees well except for the expanded area of the passband where a 0.2 dB deviation of the AIDE2 circuit is compared with the 0.05 dB deviation of the HC5512A. The simulation differs from both experimental responses on this scale. The reason for this discrepancy has not been identified. The lack of a ripple in the AIDE2 experimental or simulated response would suggest that the original design specifications which were taken from Harris engineering data may be different from what is actually used in the HC5512A. The comparison in PSRR is reasonable among all three responses. The simulated noise is almost 20 dB too small. This may be caused by higher frequency noise being folded into the passband and by ignoring the kT/C noise of the switched capacitors. One possible solution is have multiple noise sources interfaced with the appropriate length transmission line to represent the influence of the higher frequency folded noise contributions.

These results indicate that CAD techniques can be used to successfully design complex analog circuits such as switched capacitor filters. The second-order performance such as noise and PSRR is also comparable with custom designed ICs. The nonlinear effects that lead to harmonic distortion were not simulated nor was the influence of switch feedthrough considered.

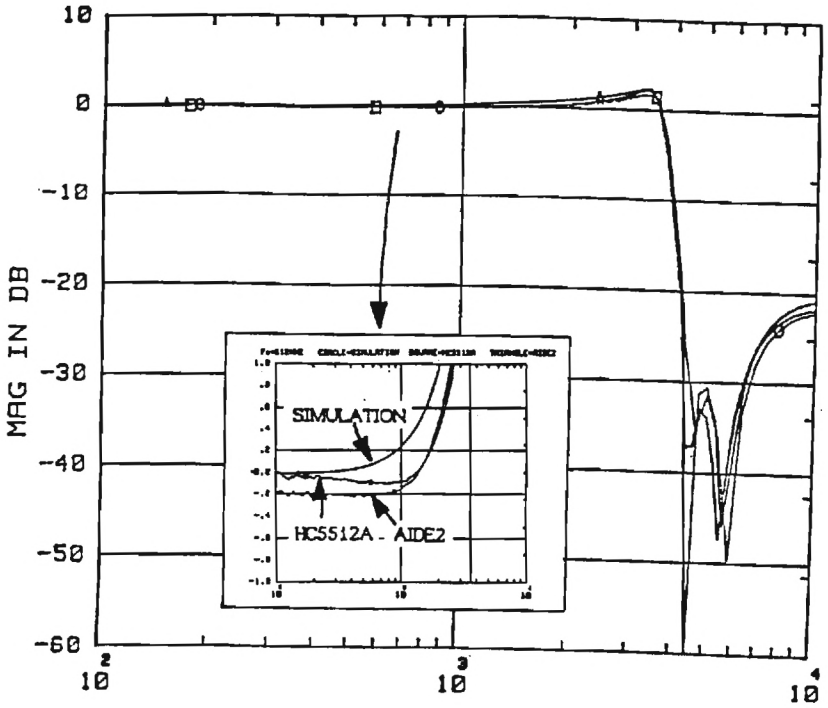


Fig. 6 - Frequency response of fifth-order, low-pass filter.

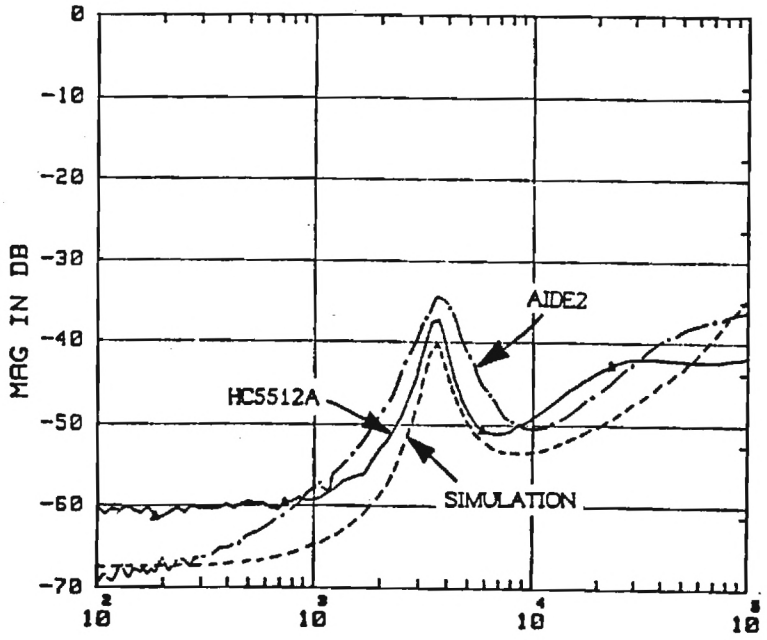


Fig. 7 - Power supply rejection ratio of the fifth-order, low-pass filter.

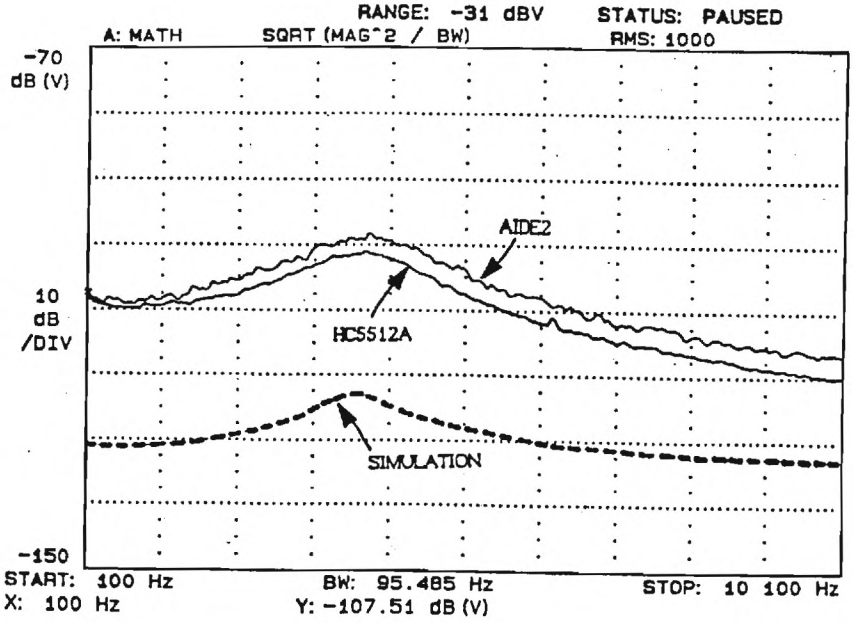
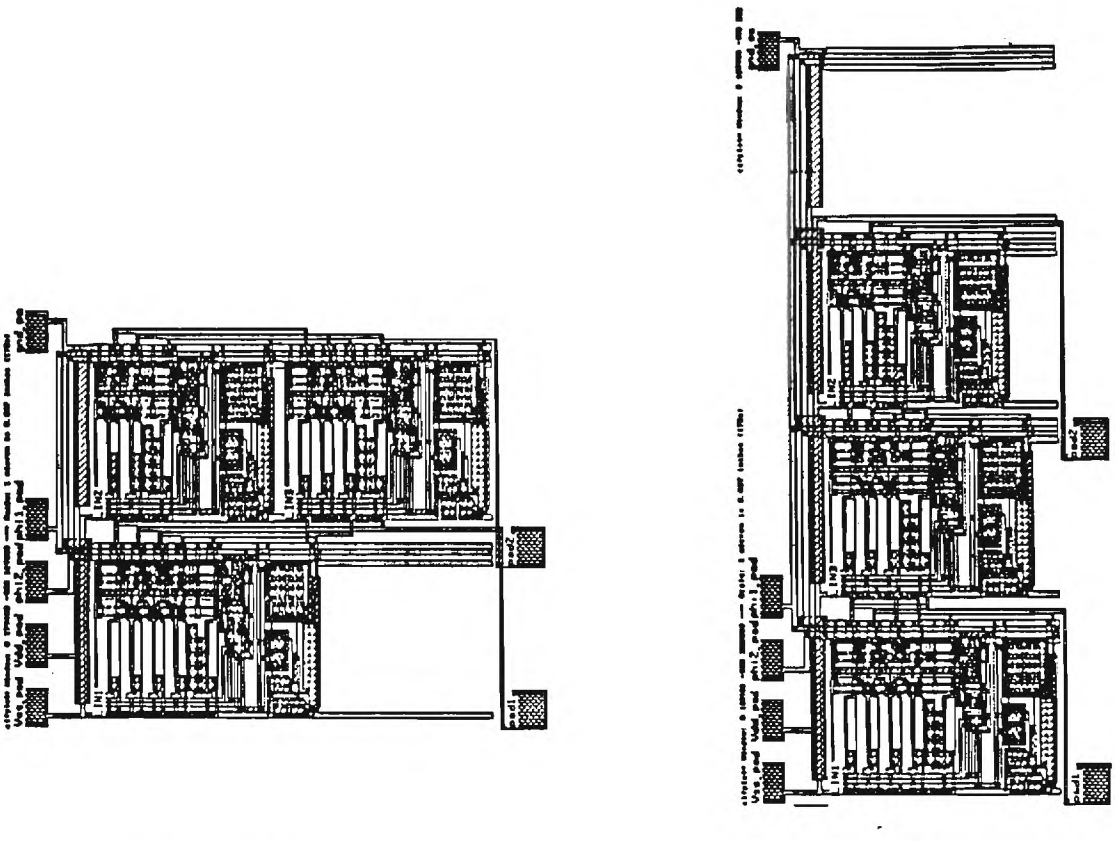


Fig. 8 - Noise performance of the fifth-order, low-pass, filter.

2.2 Comparison of Electrically Identical-Physically Different Circuits Designed by AIDE2.

The objective of this research was to identify the aspects of analog CAD techniques which limit the performance of circuits designed using these CAD techniques. AIDE2 was used to design three electrical identical third-order filters that had distinctly different layouts. Any difference in performance should be due to the physical differences of the filters. Fig. 9 shows the three layouts of elliptic, 0.1dB, low-pass filters. These filters were fabricated using the Harris SAJI IV CMOS technology. The filters are identified as FIL3 (aspect ratio = 200), FIL3N (aspect ratio = 100), and ELIPEX (aspect ratio of 50). Aspect ratios of 100 are square. Aspect ratios greater than 100 are tall and thin and aspect ratios less than 100 are short and wide.



a.) Filter 3N

b.) Fil3

c.) Elipex

Fig. 9 - The physical layout of three electrical identical filters. a.) FIL3N, b.) FIL3, and c.) ELIPEX.

Three filters of each type at various locations on the wafer were measured experimentally. The experimental results for each of the three filters was averaged and compared with the simulated data. No differences were observed until the clock frequency was increased beyond 1MHz. The filter was originally designed to have a cutoff frequency of 3.46KHz when the clock is 100KHz. The experimental data for clock frequencies above 1MHz differed for each type of filter but did not compare well with the simulated data. It was concluded that two problem exist. The first is that sample of three filter each was not large enough. Secondly, the simulation does not incorporate any of the nonideal aspects of the circuit that would be due to layout.

Effort was then made to extract the routing parasitics of each filter in order to try to get the simulation results to agree with the experimental results. Table 1 shows the extracted parameters of the three filters for routing resistance. The major difference noted is that FIL3 has 90 ohms of resistance in the ground bus and each linear block ground. FIL3N was observed to have 90 ohms of resistance between the ground buss and linear block 1. Closer inspection of Fig. 9b showed that when there is more than one row, that it becomes

Extracted Parasitic		FIL3N (R=100)	ELIPEX (R=50)	FIL3 (R=200)
VIN-LIB1	Ohms	2054	933	2300
	fF	320	205	285
LIB3-VOUT	Ohms	2026	998	2300
	fF	1740	1390	1950
GRD-LIB1	Ohms	90	1	90
GRD-LIB2	Ohms	1	1	90
GRD-LIB3	Ohms	1	1	90

Table 1 - Extracted buss resistance and capacitance of Fig. 9.

necessary for one of the power busses to cross under the other. AIDE2 was designed so that the ground bus crossed under V_{SS}. This cross under was done in diffusion and accounts for the 90 ohms.

The plans for this research are to examine the filters in the time domain so that the parasitics can be included within the simulation models easier. This means that the experimental data will also have to be retaken in the time domain. We propose to use the step response in this effort.

2.3 Measurement and Simulation of ADDAC

Another research effort in the area of performance oriented CAD techniques is the measurement and simulation of a successive approximation, analog-to-digital converter fabricated by the ADDAC compiler. Early results of this compiler did not work due to a combination of layout, design, and compiler software errors. A second fabrication was made using the MOSIS, double-poly, 3 micron, CMOS process. While five circuits were submitted, only three circuits, an 8-bit A/D, the B successive-approximation-register (SAR_B), and a comparator were accepted for fabrication because of space limitations. The SAR_B and comparator were measured and performed according to specifications. The 8-bit A/D did not work because of a software error which shifted the entire switch array down and over by 2 lambda. This in turn caused an overlap between the power busses and ground. Microsurgery was performed using an acoustical cutting probe and the short circuit was eliminated at the cost of the least significant bit of resolution. However, a fatal error was discovered as a result of the software problem. Two ports were connected via two polysilicon runs which were shorted together by the shift. This was not correctable through microsurgery techniques because the polysilicon was not the top layer. There was also a layout error in which two latches in the sar_A cell had no V_{DD} connection. Along

with the previous mentioned problems were random processing errors, all of which were shorts between two parallel metal runs. These errors proved to be the most frustrating to deal with because of the time necessary to discover them and the uncertainty of there influence.

The software and the layout errors were corrected however, it was obvious that the circuit must be totally simulated before attempting a third fabrication. Extensive efforts were made to simulate an 8-bit, successive approximation, A/D converter. IG_SPICE [4] was used to simulate a 4-bit A/D. The comparator was modeled both at the transistor level and a macromodel level. After a great deal of effort, successful simulation was achieved and revealed several design errors. These errors included: 1.) A RS flip-flop had an undefined state during power-up which charges up the capacitor array to an erroneous voltage, 2.) because this condition was not expected there was no way for the capacitor array to discharge before the conversion began causing the result to be wrong, and 3.) the accuracy of the converter was limited by the fact that throughout the circuit many pass transistors were used which consisted of a single n or p type MOS device and caused threshold errors.

The first two errors were corrected in the simulation by delaying the signal controlling a toggle switch connecting the bottom side of the capacitor array from ground to the input voltage. This allows time for the top plates of the capacitors to be shorted to ground and thereby shorting all capacitors. The third error was remedied by replacing each single device, pass transistor with a CMOS transmission gate. Simulation verified that the errors were removed. The modifications were consequently made to the ADDAC program and a 10-bit, successive approximation converter was designed by ADDAC. The layout was verified using MAGIC [5]. This 10-bit converter and a 1-bit test circuit are

being fabricated by the Harris Semiconductor Corporation.

2.4 Automated Analog Cell Compiler

The objective of this research is to develop a compiler which can generate a layout given a SPICE input file and information on the technology. Furthermore, this research has the objective of using sensitivity and knowledge of proper analog layout techniques to achieve a layout having the best analog performance. The unique aspect of this research is the use of circuit sensitivity with respect to all routing parasitics to achieve the best user-specified performance possible.

The initial effort was devoted to quantifying the influence of the layout parasitics on analog circuit performance. Perturbations in resistive and capacitive parasitics showed that significant influence was possible [6]. This result was also confirmed using the dc sensitivity option of SPICE and is illustrated in Fig. 10. It was observed that resistance parasitics between the source of a device and an ac ground and parasitic capacitances at a high

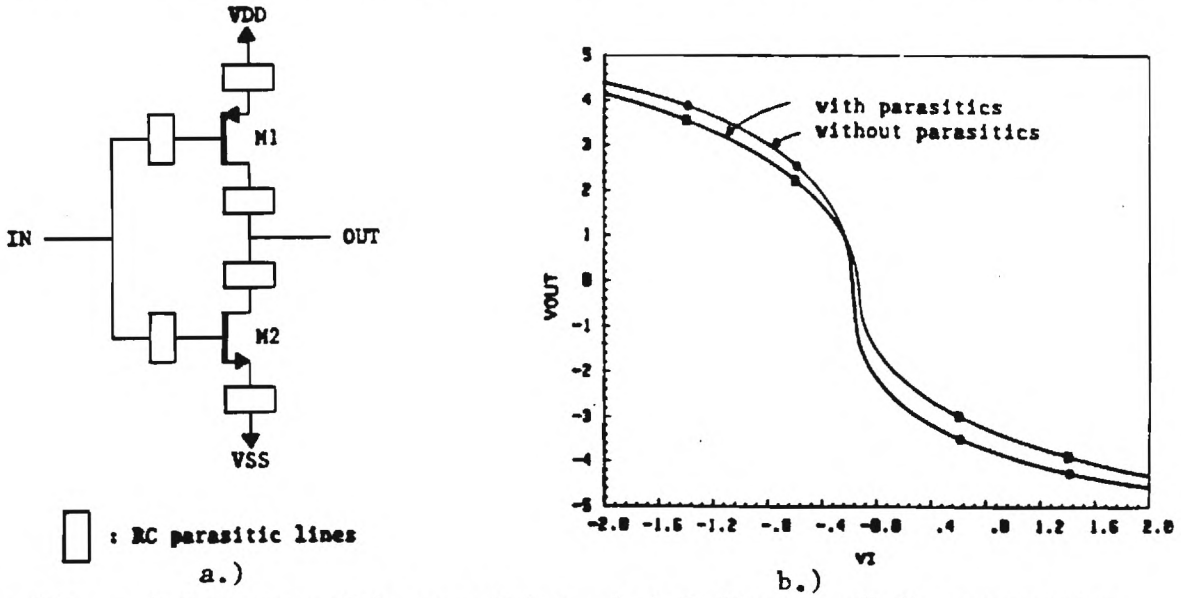


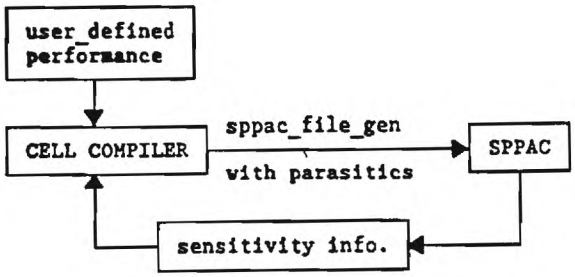
Fig. 10 - a.) Inverter with parasitics. b.) Influence of the parasitics.

impedance point were the most detrimental on the dc and ac performance.

To date the accomplishments on the analog cell compiler include the development of a device generator and the capability to perform efficient and quick ac sensitivity using SPICE. The primitives of the device generator are transistors. The transistors primitives are designed to minimize their intrinsic resistance and capacitance parasitics. As the W/L value becomes large, the generator will parallel structures to achieve a more uniform area usage. Capacitors using devices can also be employed.

Once the device physical structures are generated, then it is necessary to decide how to place them. Several algorithms are being examined for this purpose. One algorithm traces the electrical path from positive to negative power supply. Another examines the number of common nodes between devices and makes conclusions on the degree to which devices must be matched. This information is coupled with the sensitivity information to determine the optimum placement.

The sensitivity analysis is implemented in the compiler by first adding a pi-element consisting of a shunt capacitor, series resistance, and a shunt capacitor representing the parasitic of each device node. Fig. 10a shows where these parasitic RC circuits would be placed in a simple inverter. The values of the parasitic elements are not known but are given values which might be representative of the actual case. Next, dc or ac sensitivity is performed with respect to these parasitic elements to identify the important parasitic elements. The sensitivity analysis is done using SPICE-PAC [7] which is a segmented version of SPICE especially adapted to perform operations such as sensitivity. The interface of SPICE-PAC with the analog cell compiler and the output of the sensitivity analysis for dc and ac is shown in Fig. 11.



a.)

***** DC SENSITIVITIES

	ELEM	V(7)
S/RM1d	1.00d+02	-1.41d-03
S/RM1g	1.00d+02	0. d+00
S/RM1s	1.00d+02	-1.10d-01
S/RM2d	1.00d+02	1.41d-03
S/RM2g	1.00d+02	0. d+00
S/RM2s	1.00d+02	1.10d-01
S/RM3d	1.00d+02	3.59d-02
S/RM3g	1.00d+02	3.59d-02
S/RM3s	1.00d+02	2.21d-01
S/RM4d	1.00d+02	-1.02d-03
S/RM4g	1.00d+02	1.38d-15
S/RM4s	1.00d+02	-2.26d-01
S/RM5d	1.00d+02	3.85d-05
S/RM5g	1.00d+02	0. d+00
S/RM5s	1.00d+02	4.06d-03
S/RM6d	1.00d+02	2.71d-05
S/RM6g	1.00d+02	2.30d-17
S/RM6s	1.00d+02	9.49d-03
S/RM7d	1.00d+02	-3.20d-03
S/RM7g	1.00d+02	0. d+00
S/RM7s	1.00d+02	-6.46d-03
S/RM8d	1.00d+02	3.50d-05
S/RM8g	1.00d+02	3.50d-05
S/RM8s	1.00d+02	2.10d-04
S/RM9d	1.00d+02	-3.03d-04
S/RM9g	1.00d+02	-3.03d-04
S/RM9s	1.00d+02	-1.58d-03
S/RM10d	1.00d+02	2.63d-18
S/RM10g	1.00d+02	0. d+00
S/RM10s	1.00d+02	0. d+00

dc for offset

***** AC SENSITIVITIES

FREQ	S(RM1d).M	S(RM1g).M	S(RM1s).M	S(RM2d).M	S(RM2g).M	S(RM2s).M
1.00d+00	2.22d-05	1.00d-20	2.90d-03	2.90d-05	2.29d-10	2.57d-03
1.00d+01	2.22d-05	2.63d-10	2.90d-03	2.90d-05	2.29d-07	2.57d-03
1.00d+02	2.22d-05	2.63d-07	2.90d-03	2.31d-05	2.29d-06	2.57d-03
1.00d+03	2.24d-05	2.67d-06	2.91d-03	2.32d-05	2.29d-07	2.58d-03
1.00d+04	2.28d-05	2.72d-07	2.93d-03	2.37d-05	2.27d-06	2.63d-03
1.00d+05	2.29d-05	2.68d-06	2.82d-03	4.01d-05	2.23d-05	3.14d-03
1.00d+06	2.43d-05	2.75d-05	1.86d-03	1.16d-04	2.31d-04	9.18d-03

FREQ	S(RM3d).M	S(RM3g).M	S(RM3s).M	S(RM4d).M	S(RM4g).M	S(RM4s).M
1.00d+00	6.20d-04	6.20d-04	9.04d-03	2.38d-05	1.00d-20	9.27d-03
1.00d+01	6.20d-04	6.20d-04	9.04d-03	2.57d-05	1.42d-09	9.27d-03
1.00d+02	6.20d-04	6.20d-04	9.04d-03	2.38d-05	1.42d-08	9.27d-03
1.00d+03	6.24d-04	6.24d-04	9.06d-03	2.36d-05	1.42d-07	9.22d-03
1.00d+04	6.35d-04	6.35d-04	9.15d-03	2.29d-05	1.41d-06	9.04d-03
1.00d+05	6.26d-04	6.26d-04	9.08d-03	2.84d-05	1.39d-05	9.01d-03
1.00d+06	6.03d-04	6.03d-04	8.72d-03	1.92d-05	7.00d-05	6.24d-03

FREQ	S(RM5d).M	S(RM5g).M	S(RM5s).M	S(RM6d).M	S(RM6g).M	S(RM6s).M
1.00d+00	1.23d-08	1.00d-20	1.30d-06	2.27d-04	4.40d-10	7.96d-02
1.00d+01	1.23d-08	1.00d-20	1.30d-06	2.27d-04	4.41d-09	7.96d-02
1.00d+02	1.23d-08	2.22d-12	1.30d-06	2.28d-04	4.41d-08	7.96d-02
1.00d+03	1.27d-08	2.31d-11	1.34d-06	2.28d-04	4.41d-07	7.96d-02
1.00d+04	2.91d-08	2.70d-10	3.07d-06	2.28d-04	4.41d-06	7.96d-02
1.00d+05	2.66d-07	1.91d-08	2.74d-05	2.92d-04	4.39d-05	7.94d-02
1.00d+06	1.94d-06	1.12d-06	2.08d-04	7.64d-04	2.22d-04	4.86d-02

FREQ	S(RM7d).M	S(RM7g).M	S(RM7s).M	S(RM8d).M	S(RM8g).M	S(RM8s).M
1.00d+00	2.67d-02	1.84d-10	5.42d-02	2.77d-13	2.77d-13	1.66d-12
1.00d+01	2.67d-02	1.84d-09	5.42d-02	2.77d-12	2.77d-13	1.66d-11
1.00d+02	2.67d-02	1.84d-08	5.42d-02	2.77d-11	2.77d-11	1.66d-10
1.00d+03	2.69d-02	1.84d-07	5.42d-02	2.75d-10	2.75d-10	1.63d-09
1.00d+04	2.69d-02	1.84d-06	5.42d-02	2.67d-09	2.67d-09	1.61d-08
1.00d+05	2.68d-02	1.83d-05	5.42d-02	2.63d-08	2.63d-08	1.58d-07
1.00d+06	2.62d-02	1.80d-04	5.30d-02	1.41d-07	1.41d-07	8.49d-07

FREQ	S(RM9d).M	S(RM9g).M	S(RM9s).M	S(RM10d).M	S(RM10g).M	S(RM10s).M
1.00d+00	2.08d-11	2.08d-11	1.09d-10	8.84d-20	1.00d-20	1.30d-14
1.00d+01	2.08d-10	2.08d-10	1.09d-09	8.84d-18	4.69d-16	1.31d-12
1.00d+02	2.08d-09	2.08d-09	1.09d-08	8.82d-16	8.06d-14	1.32d-10
1.00d+03	2.06d-08	2.06d-08	1.08d-07	6.46d-14	5.23d-11	1.04d-08
1.00d+04	2.01d-07	2.01d-07	1.05d-06	3.09d-13	2.34d-09	4.63d-08
1.00d+05	1.78d-06	1.78d-06	1.03d-05	2.63d-12	2.92d-08	6.41d-08
1.00d+06	1.06d-05	1.06d-06	8.85d-05	2.80d-11	8.53d-07	9.00d-07

ac for gain bandwidth

b.)

Fig. 11 - a.) Interface of SPICE-PAC with the analog cell compiler. b.) Output of the sensitivity analysis for dc and ac sensitivities.

The use of sensitivity allows the compiler to select placement and routing strategies which can optimize the performance of the analog circuit. The user can input one or more performances of the circuit which must be optimized with respect to layout. Sensitivity permits the implementation of this capability.

The plans for the analog cell compiler include interfacing the routing and

placement constraints with the placement and routing implementation. The router MIGHTY [8] will be used. Iterations in the device generation and placement are expected as the program progresses to a final layout. A working prototype compiler is expected in early 1989.

3.0 MULTILEVEL ANALOG AND ANALOG-DIGITAL SIMULATION TECHNIQUES

The development of analog silicon compilers such as ADDAC and AIDE2 have demonstrated the important need of simulation capability for complex circuits containing both analog and digital parts. This research initially was oriented toward the development of a multilevel analog simulator [9]. However, with the availability of SABER [10] the focus has turned to the evaluation of mixed analog-digital simulation and higher level modeling for analog circuits. The objective was twofold. The first objective was to determine if present commercially available mixed analog-digital simulators are adequate for complex analog and digital circuits. The second objective was to develop modeling methods of making the analog part of mixed analog-digital simulators more efficient. The results of this research are divided into the categories of evaluation of two mixed analog-digital simulators, macromodeling for complex nonlinear circuits and systems, and automatic behavioral model generation.

3.1 Evaluation of IG_SPICE and SABER.

The objective of this research was to evaluate the capabilities of IG_SPICE and SABER as multilevel and mixed analog-digital simulators. Because the successive approximation A/D converters described earlier in this report needed to be simulated, this circuit was selected as the example to be tried. Furthermore, the presence of partially working integrated circuits provided a means of confirming the simulation.

Because IG_SPICE was available elsewhere on campus it was used first while

SABER was being purchased and personnel trained. IG_SPICE is categorized as an analog simulator extended to incorporate digital macromodels. A simplified diagram of the converter is shown in Fig 12. Initially the converter was simulated part by part and then combined to a 4-bit, successive approximation, A/D converter. Both dc and transient analyses were performed. The modeling level varied from individual devices for switches and passive components to macromodels for the comparator and logic circuits.

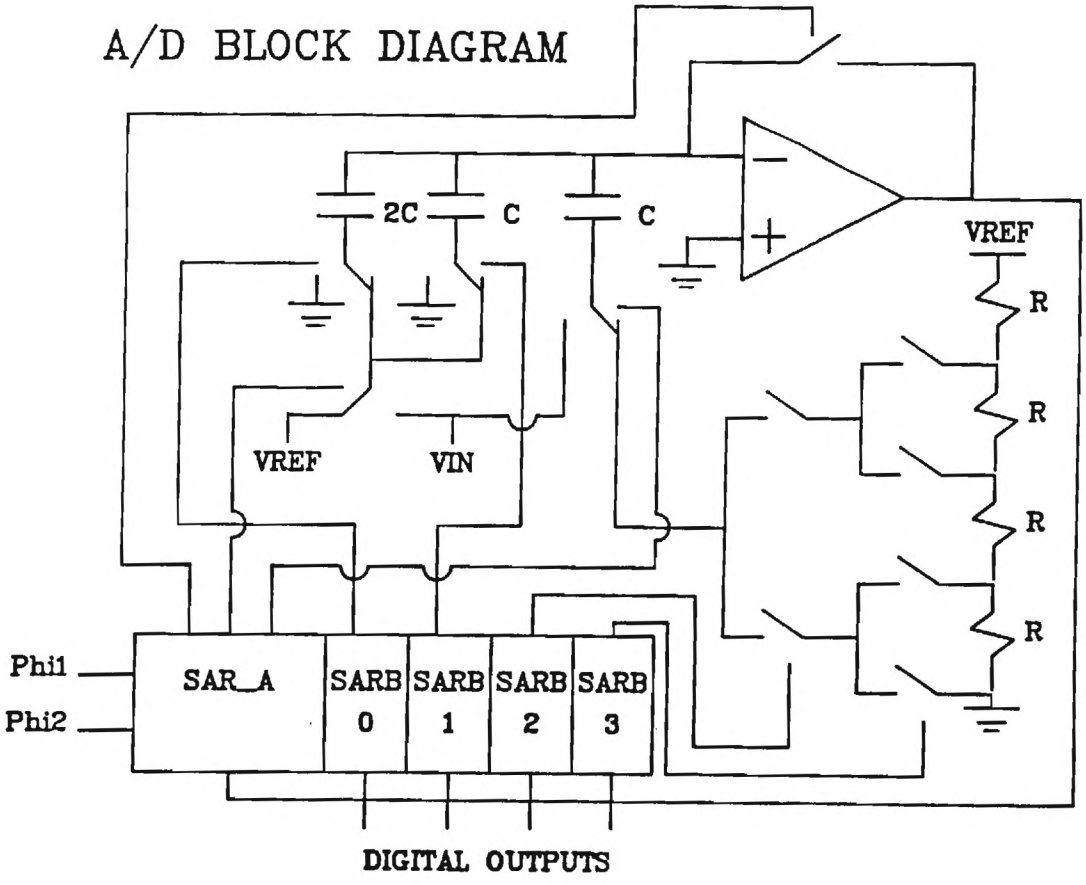


Fig. 12 - Simplified block diagram of the succ. approx. A/D converter.

Successful results were obtained after several problems were solved. These

problems included the usual problems in dc convergence, timing problems resulting from the use of ideal digital elements, and problems resulting from design errors. The careful use of NODESET options, the addition of time delay to the gates, and correct circuit configurations resulted in successful simulation. A typical 4-bit converter transient analysis took 4-6 hours on an Apollo 3000.

The successive approximation A/D converter was simulated using SABER which is also an analog simulator extended to include digital models. Considerable difficulty was experienced in learning how to use SABER for simulation. Most of the difficulties were encountered in developing digital models. Several digital gate behavioral models were developed in the MAST modeling language of SABER. These gates included an AND and NOR gate, an inverter, and a D latch with/without a reset signal. A switch behavioral model was also developed. With these models and others from the SABER template library, the SAR_A and SAR_B were successfully simulated but the total 4-bit converter was not successful. (At the time of writing this report, the 4-bit converter has been successfully simulated by SABER and took 1.5 hours on a MicrovaxII. The model levels are comparable to those of the 4-6 hour simulation of IG_SPICE on the same circuit.)

During the summer of 1988, the opportunity to evaluate another potential mixed analog-digital simulation capability was available. This simulator was a version of SPICE-PAC containing table driven models. The analog-digital interface is illustrated in Fig. 13. No timing information is permitted in the digital models although a delay can be introduced in the digital to analog conversion aspect. With the logic modeled at the logic level (Boolean equations), the simulation of a 4-bit and 8-bit successive approximation A/D converter took 21 and 35 minutes respectively.

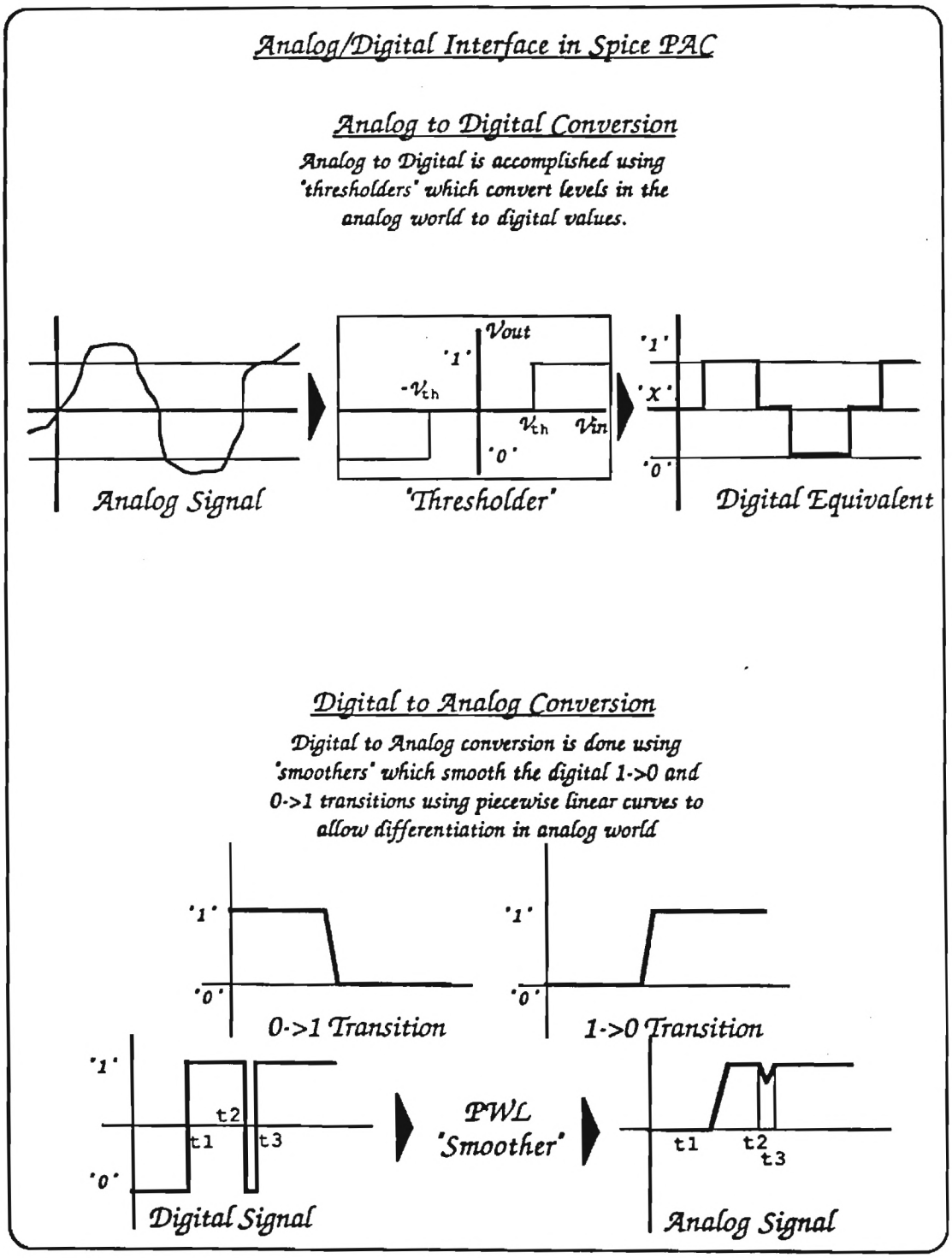


Fig. 13 - Illustration of the Analog-Digital Interface in SPICE-PAC.

The plans for this study include completing the 4-bit converter simulation by SABER, comparing SPICE-PAC with SABER and IG_SPICE using equivalent modeling levels, and extending the capability of SPICE-PAC to include timing information for the logic simulation. The timing interface of SPICE-PAC will allow the coupling of SPICE-PAC with a digital simulator at the timing level and should permit an efficient coupling of the two simulators to form a true, mixed analog-digital simulator.

3.2 Macromodeling for Complex Nonlinear Circuits and Systems

The need for higher level modeling has resulted in two different approaches. The one described in this subsection uses SPICE primitives and is implemented on the SPICE simulator. For purposes of notation, this type of modeling will be called macromodeling. A functional macromodel for a voltage controlled oscillator (VCO) and a phase detector have been developed. These models use blocks such as a multiplier, integrator, triangle-to-sine converter, sine-to-square converter and a schmitt trigger. The models are capable of any SPICE analysis including linear and nonlinear. The VCO and phase detector have been combined to realize an analog phase-locked loop (APLL) shown in Fig. 14.

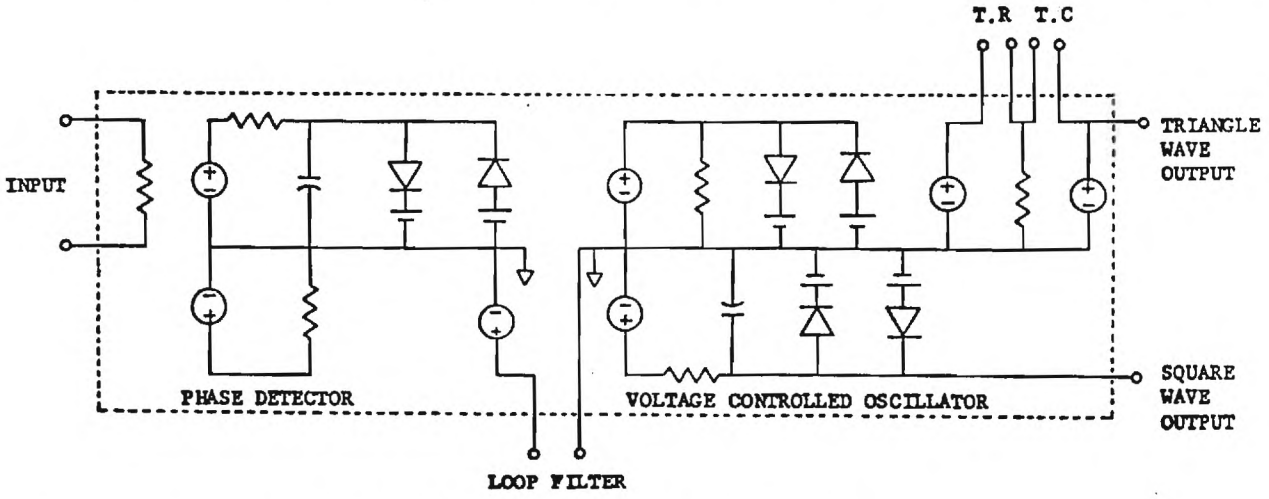


Fig. 14 - A macromodel of an analog phase-locked loop.

The performance of this macromodel is illustrated in Fig. 15 where the output voltage of the loop filter is shown for a frequency sweep rate of 55 Hz/ms. The simulation was performed using PSPICE on a personal computer and took approximately 2 hours. The results have been compared with theoretical expectations and agree closely. A macromodel for continuous and discrete time filters has been developed in order to complete the APLL model. A device level simulation of the APLL by SPICE will be performed in order to evaluate the macromodel performance. Other aspects such as noise and temperature dependence of the APLL will also be modeled.

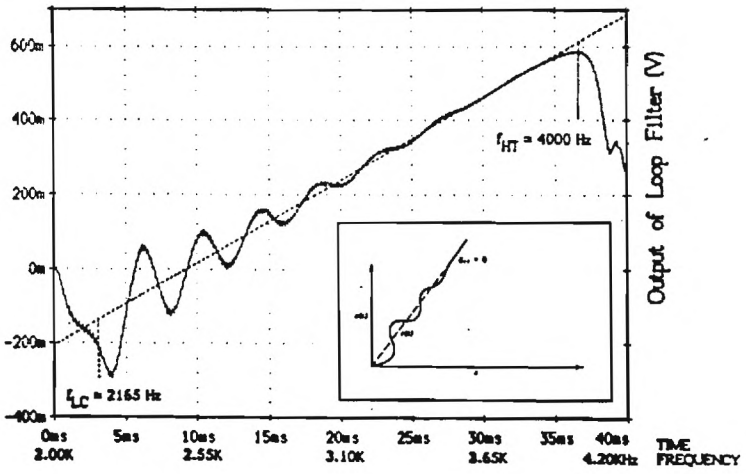


Fig. 15 - Output voltage of the loop filter of the analog phase-locked loop.

3.3 Automatic Behavioral Model Generation

The second higher level analog modeling effort is the analog behavioral modeling effort described in this subsection. This research has the objective of developing behavioral models of analog circuits which preserve as much accuracy as possible and minimize simulation time. The automatic generation of

these models is also an objective.

The preliminary work began with a personal survey of how mixed analog-digital simulation was accomplished in 10 SRC member companies. The results of this survey were published in an SRC document [11]. In essence, the survey found the problem to be of extreme importance with no generally accepted solution available. IG_SPICE, SABER, LSIM, and MIXsim are simulators being used for mixed analog-digital simulation with varying degrees of success. Based on this survey and the advent of commercial software such as SABER, it was decided to focus upon behavioral modeling for analog circuits. This involved attending a week-long training course on SABER and innumerable hours spent learning how to correctly use the SABER simulator.

In order to understand the problem of behavioral modeling of analog circuits, it was decided to develop a behavioral model of an analog comparator. Behavioral modeling is a loosely defined term but here it is taken to mean the use of equations implemented in FORTRAN, C, or in the case of SABER in the MAST modeling language. Therefore, a simulator having behavioral modeling capability by this definition must have the ability to accept a language description of the model.

The initial behavioral modeling attempts consisted of routines implemented in the C programming language which extracted the dc and transient characteristics of an analog voltage comparator, with or without hysteresis, from SPICE or experimental results and converted these characteristics into a SABER comparator template (model) for subsequent use in a simulation using the SABER platform. At the present, the SABER templates are not automatically generated. The default parameters are simply written into the model. However, the purpose at this point was to determine the capability of the modeling methodology.

The simulation of the analog comparator using SABER and the behavioral model was compared with SPICE using device level models. The dc transfer characteristic modeled by a three-segment, piecewise linear model was more than 10 times faster than the SPICE with transistor level models. The transient analysis showed that the model was only about 2 times faster than SPICE.

Evaluation of the above results led to a much more powerful and general behavioral modeling technique based on the concept of nonlinear, differential equations (NDEs). This modeling technique uses nodal equations at certain points in the analog circuit. Each nodal equation can have a nonlinear, multidimensional forcing function, linear and nonlinear terms, and derivatives of the voltage variables including the node voltage and other nodes. The two stage comparator used above has been completely modeled by the following two equations.

$$G_1(V_{in}) = H_1(V_1) + C_1 d(V_1)/dt \tag{2}$$

$$G_2(V_1) = H_2(V_{out}) + C_2 d(V_{out})/dt \tag{3}$$

The functions G and H are nonlinear functions represented by in this case single dimensional tables but they could easily be extended to multidimensional tables. These functions are extracted by SPICE analysis on the actual circuit. Additional nodal equations can be included to account for common mode behavior and for higher order dynamics of the comparator.

Fig. 16 shows the results of this modeling methodology. It is far superior to the initial approach employed in this subsection. Fig. 16a shows the schematic of the comparator. Figs. 16b, 16c, and 16d show the small signal, dc transfer curves, and the large signal transient analysis of the model represented by Eqs. (1) and (2). Table 2 shows the performance comparison between SPICE using device level models and SABER using the above model on a Microvax.

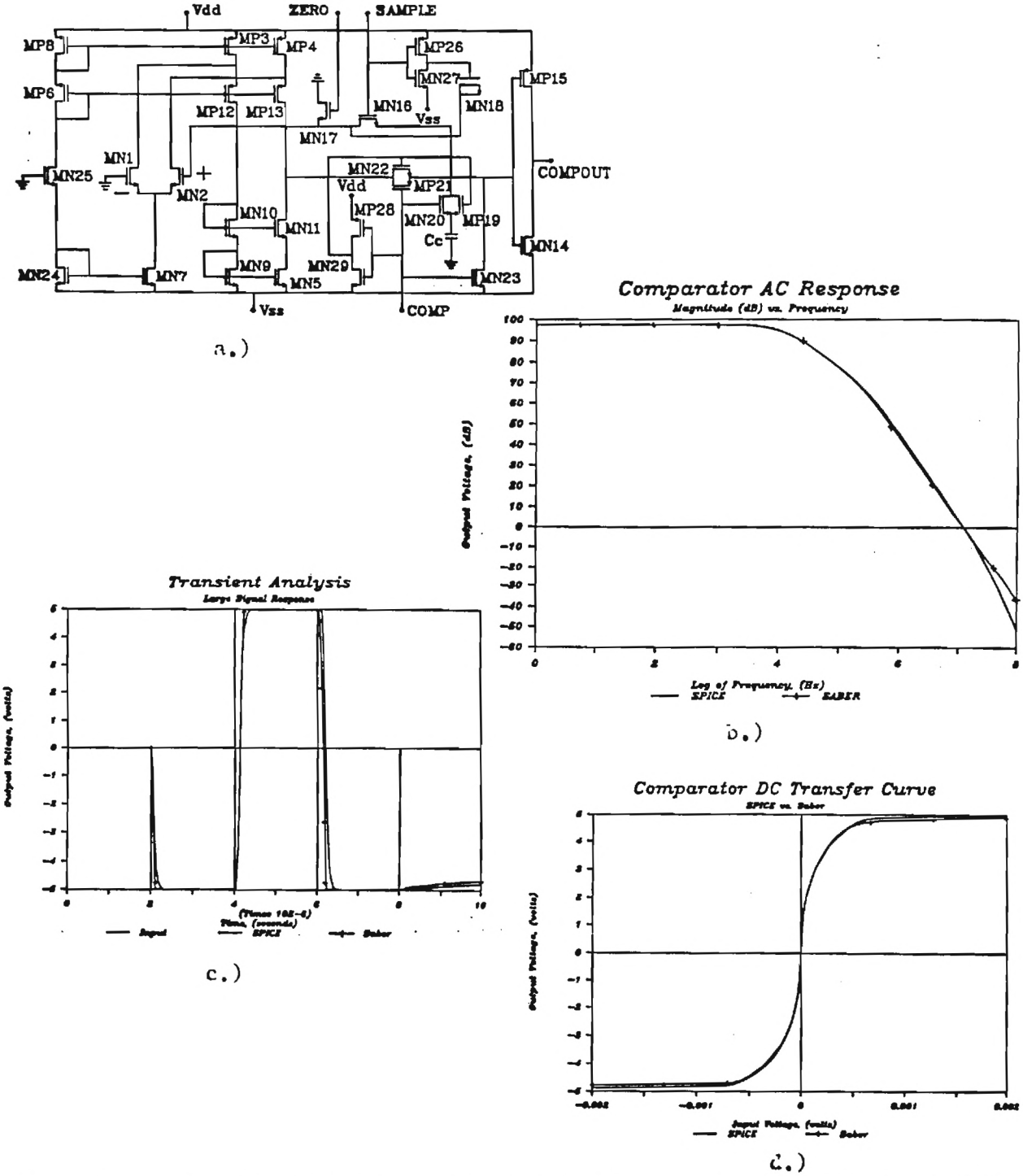


Fig. 16 - a.) Comparator schematic. b.) Comparator ac responses for SPICE and SABER. c.) Comparator dc transfer curves for SPICE and SABER. d.) Comparator transient responses for SPICE and SABER.

Analysis	SABER (uVAX seconds)	SPICE (uVAX seconds)
.OP	1.00	15.53
.DC	17.60	150.60
.AC	9.63	40.40
.TRAN	29.40	534.30
Totals	57.63	741.83

Table 2 - Comparison of simulation time for SABER and SPICE.

The results above are very encouraging, particularly since the behavioral level simulation is able to model many of the important aspects of the device level performance. For example, the delay of the comparator to an input stimulus will vary depending upon the value of the common mode signal if a third equation representing the common mode node is included.

The plans for this research are to investigate further the ability of the method to model include other performance aspects of the comparator. The behavioral model appears to have the ability to make a complexity versus speed tradeoff. After applying this methodology to a different circuit, an attempt to formalize the methodology will be made. This should lead to the desired generality leading to automatic extraction and generation of behavioral models.

4.0 PRECISION MODELS FOR ANALOG CIRCUIT DESIGN

The objective of this research effort is to develop models and a model methodology which result in computer efficient, accurate analog small signal models for short-channel MOSFETs including submicron devices. The methodology has been generalized and is extendable to MESFETs and bipolar devices. The model is particularly suited for the circumstance where increased accuracy is desired or where the device is difficult to model by normal means. The input to this program requires actual device data or a device simulator output.

The modeling methodology developed uses a table look-up (TLU) approach. At each linearly spaced value of the independent variable, the magnitude of the dependent variable is stored along with the numerically calculated slope of the dependent variable. A cubic spline interpolation scheme is used, one dimension at a time, to find the magnitude and slope of the dependent variable. The TLU has been benchmarked on single devices and circuits against the SPICE level 2 and BSIM [12] models. The benchmark results show the TLU to be approximately equivalent in dc accuracy and to have about 10 times more ac accuracy with 40% less computation time. The typical memory requirement for a single MOSFET is about 8 kbytes. The model is scalable in channel width but not in channel length.

The resolution of the TLU and BSIM models have been compared to statistical device variations is illustrated in Fig. 17. The dc and ac statistical spread of all three of the independent variables (V_{DS}, V_{GS}, and V_{BS}) are shown. The dc statistical spread for both the BSIM and TLU models is about 5% whereas the ac statistical spread for the TLU model is much less than the BSIM model. This data was taken on the MOSIS 1.6 micron, CMOS technology.

The TLU model has also been used to predict the dc and ac performance of an op amp fabricated in a 1.6 micron CMOS technology. The channel lengths were all 1.6 micron which implies effective channel lengths close to 1 micron. The channel widths varied from 1.6 to 166 microns. The op amp was a standard, two-stage, 7-transistor op amp. The average error of the open loop gain of 6 op amps was 3.7% for the TLU model and 28% for the BSIM model. The average error of the output resistance of 6 op amps was 4.8% for the TLU and 53% for the BSIM model. The CPU time for this analysis was 14.65 seconds for the TLU model and 15.15 seconds for the BSIM model.

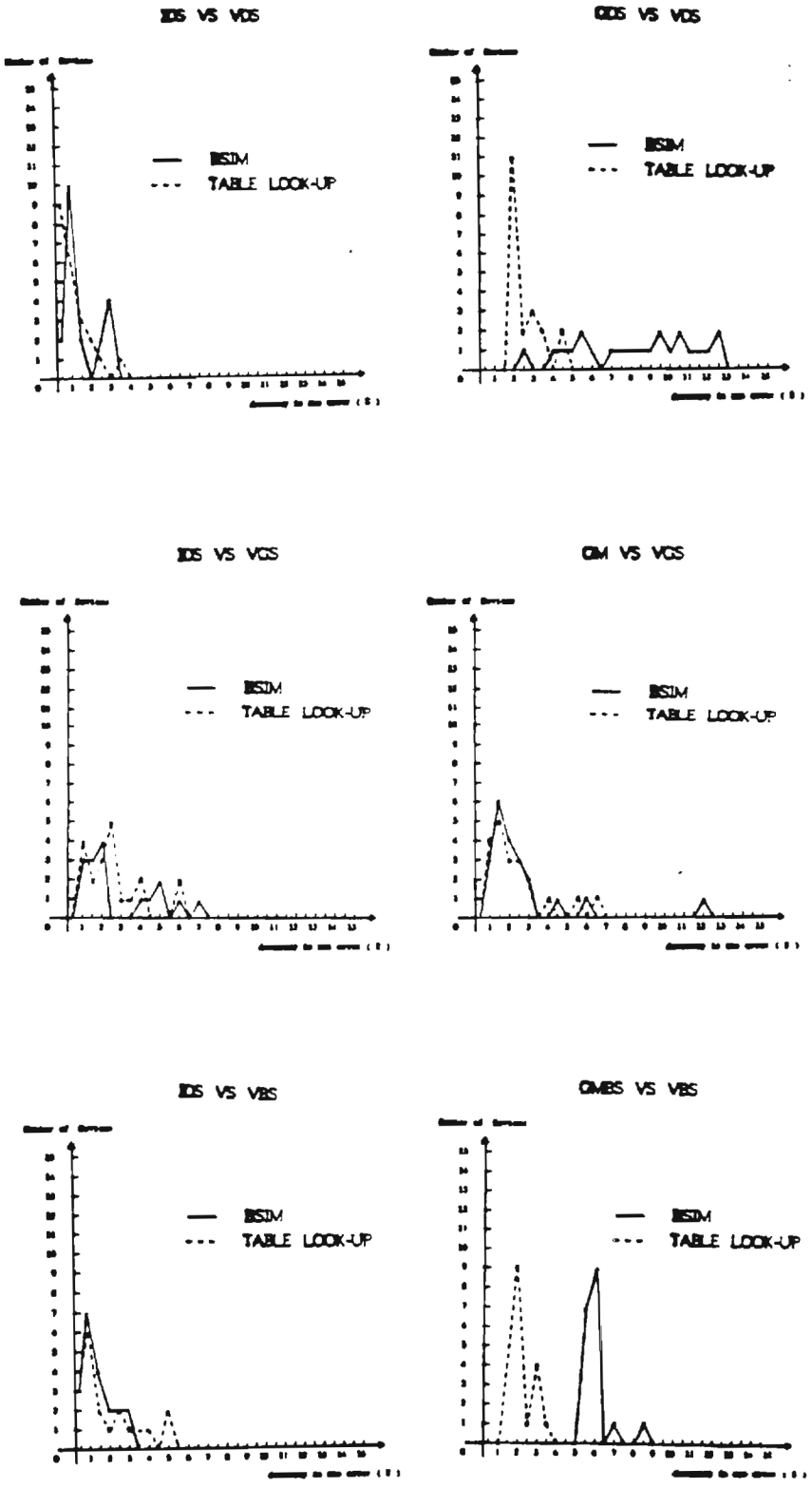


Fig. 17 - DC and ac statistical accuracy of the TLU and BSIM MOSFET models.

The TLU has been applied to a complex op amp designed by an SRC member company in 1.25 micron CMOS. Both the TLU and BSIM models were extracted and used for simulation. The BSIM model would not converge while the TLU model gave consistent results but experienced problems with some of the devices working in subthreshold. A very high gain CMOS op amp has also been designed and is being used as a benchmark for the TLU. Normal SPICE simulation give the gain of this op amp as near 10^6 whereas measurements indicate a gain of $35x10^3$. The value of r_{ds} is cubed in the gain expression and thus the open loop voltage gain is extremely sensitive to the accuracy of the small signal channel conductance.

The TLU model is presently being extended to a nonuniform spacing of the independent variables. This will allow the extraction program to extract data consistent with a user specified dc and ac accuracy. It will also permit the program to achieve accurate results both in the subthreshold and strong inversion regions. The model will be extended to include the intrinsic parasitic capacitance and generalized to the bipolar and MESFET devices. This work is expected to be complete in the summer of 1989.

5.0 AUTOMATED DESIGN TECHNIQUES

The objective of this research is the development of an automated design techniques for analog circuits. A program called AUTOAMP was developed which uses analytical expressions to design the W/L values of fixed topology op amps. This program was used to design several op amps which were fabricated and compared favorably with the specifications of the program. A second program was developed which allowed for topological choices to meet given specifications. This program picks the best structure that would attempt to satisfy user-weighted input specifications. This program has been debugged and several op amps have been designed but not submitted for fabrication. These two programs are not

being pursued further because they were used to develop experience and because more sophisticated programs for designing op amps exist.

The major research objective is the development of a program that can generate small signal designs to meet given specifications and then convert these generic small signal designs into a given technology. The program uses degenerate circuit elements and a rule-based approach to systematically generate generic circuit topologies which satisfy a two-port specification which includes a gain specification, input resistance, and output resistance. The generic realization is in terms of degenerate circuit elements and resistors. The program which implements this is called AUTOGEN.

Next, the generic realizations are converted into biasable realizations given a technology (MOSFET, bipolar, etc.). This is accomplished by a rule-base approach which recognizes biasing paths from upper power supply to lower power supply. Current sources/sinks are included where needed in order to enable a successful translation from the degenerate circuit to the transistor circuit. This part of the program is called AUTOTRAN and has been coupled to AUTOGEN. At the present time, the program works successfully but the output is hard to interpret. A schematic output with a SPICE input file is being developed in order to better interpret the output of the program and to proceed to the next step which is the refinement of the design using the SPICE simulator.

6.0 SUMMARY AND PLANS

This report has described the results of research in analog CAD methodology during the academic year, 1987-88. The objective of this research has been to develop methodologies for analog circuit design which can be implemented by the computer. The research has been devoted to improving and extending the capability of automated analog circuit design.

The research described in this report is divided primarily into the design, modeling, and simulation of analog devices, circuits, and systems as illustrated in Fig. 1. The major accomplishments of this years research are precision analog models for transistors, higher level modeling methods for analog circuits, use of various simulators to simulate complex analog-digital circuits, and a compiler for automatic layout of analog circuits. Research efforts which fell short of expectations included identification of performance limitations on AIDE2-designed circuits, the successful use of ADDAC, and the automated circuit design using generic circuit elements. New research efforts include the evaluation of SPICE-PAC as a mixed analog-digital simulator.

The first project completion will be the table look-up model for transistors. This modeling methodology has its place in new or unusual technologies where experimental data is available but models have not yet been developed or are not satisfactory. In addition, this methodology has an adjustable accuracy capability which means the model can be adjusted to the desired dc or ac accuracy. Normally, the accuracy of the model would be determined during the extraction, however, it would be possible to permit the accuracy of the model to vary during simulation. New modifications of the program will permit the model to be extremely robust and to work over very large ranges of the dependent and independent variables.

A second project that is rapidly gaining maturity is higher level modeling. Higher level modeling includes macromodeling and behavioral modeling. The macromodeling project should be completed during 1989 after an analog phase-locked loop has been successfully simulated and benchmarked. A great deal of effort is presently being spent on benchmarking a device level simulation with a macromodel simulation.

The initial mixed analog-digital simulation investigations showed that behavioral modeling was a more appropriate research topic than the development of a mixed analog-digital simulator. This has led to the development of a behavioral modeling methodology based on nonlinear differential nodal equations. The methodology provides a complete large signal and small signal time and frequency domain modeling capability. It has been applied to a complex comparator with accuracies that can approach device level simulation and CPU times of an order of magnitude smaller. The nonlinear differential equations are implemented into any simulator having the ability to accept languages and where the derivative can be defined. This modeling methodology has an adjustable level of accuracy in the sense that the methodology selects the most important nodes only. If further accuracy is desired, some of the less important nodes can be included in the model. Each node represents an additional nodal equation.

The behavioral model research is presently being applied to an op amp. Significantly different results have been obtained compared with the comparator. Once the op amp is complete and benchmarked, the methodology will be generalized so that automatic behavioral model generation capability can be realized. This project is planned for completion in early 1990.

Excellent preliminary results have been obtained for the compiler to automatically layout analog circuits. The use of sensitivity in placement and routing allows the compiler to optimize the layout according to user specified performance requirements. This program uses a version of SPICE-PAC which includes both ac and dc sensitivities. The ac sensitivity is accomplished by the adjoint method. This program has been used to place the devices in a manner which is electrically and physically efficient. The routing of the devices is the next task with possible iteration in the placement being required. A

preliminary version of the program with examples and documentation will be available in the spring of 1989. The program will be extended to include analog arrays (placement will be selection of fixed devices) and should be complete in early 1990.

The efforts to determine the performance limits of circuits and systems designed by AIDE2 and ADDAC will continue but will be given secondary importance. The 10-bit successive approximation analog-digital converter designed by ADDAC and presently in fabrication will be tested and documented. The automated design of analog circuits using generic circuit elements will also continue but the student who is doing this research is leaving school for several quarters which will cause a hiatus in this research until late 1989. Anticipated completion date of the automated design technique would be late 1990.

A new area was examined during the summer of 1988. This area is an outgrowth of the mixed analog-digital simulation performed by IG_SPICE and SABER. Dr. Wlodek Zuberek from the Computer Science Department of the Memorial University of St. John's, Newfoundland was working with our SRC group this past summer in order to develop the ac sensitivity in SPICE-PAC. Dr. Zuberek is the developer of SPICE-PAC and said that it would be capable of mixed analog-digital simulation. Preliminary investigations confirmed this and present are directed to demonstrating the capabilities of SPICE-PAC as a mixed analog-digital simulator. The plans are to install a coordinated timing interface into SPICE-PAC and to connect SPICE-PAC with an appropriate digital simulator. An "appropriate digital simulator" is one where we have access to the source code and is a multilevel digital simulator. This activity will take place in the spring of 1989 and the evaluation of SPICE-PAC should be complete at the end of the summer 1989. At this point it should be apparent whether or not to continue

this research.

The anticipated dates of task completions are summarized below for convenience. These dates may vary due to personnel and technical uncertainties.

Task Description	Student	Completion Date
Precision models for analog design	Yoon	Summer 1989
Macromodeling of Complex Analog Circuits	Choi	Fall 1989
Behavioral Modeling of Analog Circuits	Mantooth	Spring 1990
Analog layout compiler	Hong	Winter 1990
Evaluation of CAD performance limits	Li	Summer 1989
Evaluation of ADDAC 10-bit, A/D converter	Li	Summer 1989
Automated Analog Design	Loo	Fall 1990
Evaluation of SPICE-PAC as a mixed analog-digital simulator	Yan	Summer 1989

Table 3 - Anticipated completion dates of research tasks.

As the research described matures, the objective will be to more strongly focus the research activities into areas where expertise has been developed. These areas are higher level modeling, mixed analog-digital simulation, and automated design and testing. Cooperative efforts with industry and other SRC university research groups will be continued in order to conserve research resources. For example, it appears that mixed analog-digital simulation research at CMU would be appropriate for our behavioral modeling and may provide the best answer to mixed analog-digital simulation. The analog testability issue is one of strong importance and the higher level modeling and mixed analog-digital simulation experience will be very important in looking for solutions to this problem. It is felt that testability and total simulation are very closely coupled.

8.0 ACKNOWLEDGEMENTS

The amount of research undertaken in this report requires extensive cooperation and resources of those outside of the university. The following acknowledgments are gratefully made: the fabrication resources provided through the efforts of Tom Haycock at Harris Semiconductor, the linear CMOS arrays and design information provided by Greg Winner of Silicon Systems, resources and design information from Scott Marin of Texas Instruments, and many discussions, information, and encouragement from Miran Milkovic of General Electric. The internal resources of the Schlumberger Chair and University Research Funds are also acknowledged.

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